

COMPAL CONFIDENTIAL

MODEL NAME : NCL00 NCL10(ATG)

PCB NO : LA-5471P ( DA80000G710)

E2 Rothschild UMA

rPGA Arrandale +  
FCBGA PCH IBEXPEAK-M

2010-1-20  
REV : 1.0(A00)

@ : Nopop Component

MB Type	BOM P/N	PCMCIA	Express	TCM		TPM				ATG	BOM CONFIG
		1@	2@	W(3@)	W/O(4@)	W(5@)	W/O(6@)	7@	8@	9@	
PCMCIA CARD EN,TPM EN,TCM DIS	43177931L11	*			*	*					1@,4@,5@
EXPRESS CARD EN,TPM EN,TCM DIS	43177931L14		*		*	*					2@,4@,5@
PCMCIA CARD EN,TCM EN,TPM DIS	43177931L12	*		*			*				1@,3@,6@
EXPRESS CARD EN,TCM EN,TPM DIS	43177931L15		*	*			*				2@,3@,6@
PCMCIA CARD EN,ALL TPM DISABLE	43177931L13	*			*		*				1@,4@,6@
EXPRESS CARD EN,ALL TPM DISABLE	43177931L16		*		*		*				2@,4@,6@
PCMCIA CARD EN,TPM EN,TCM DIS	43177931L01	*			*	*				*	1@,4@,5@,9@
PCMCIA CARD EN,TCM EN,TPM DIS	43177931L02	*		*			*			*	1@,3@,6@,9@
PCMCIA CARD EN,ALL TPM DISABLE	43177931L03	*			*		*			*	1@,4@,6@,9@

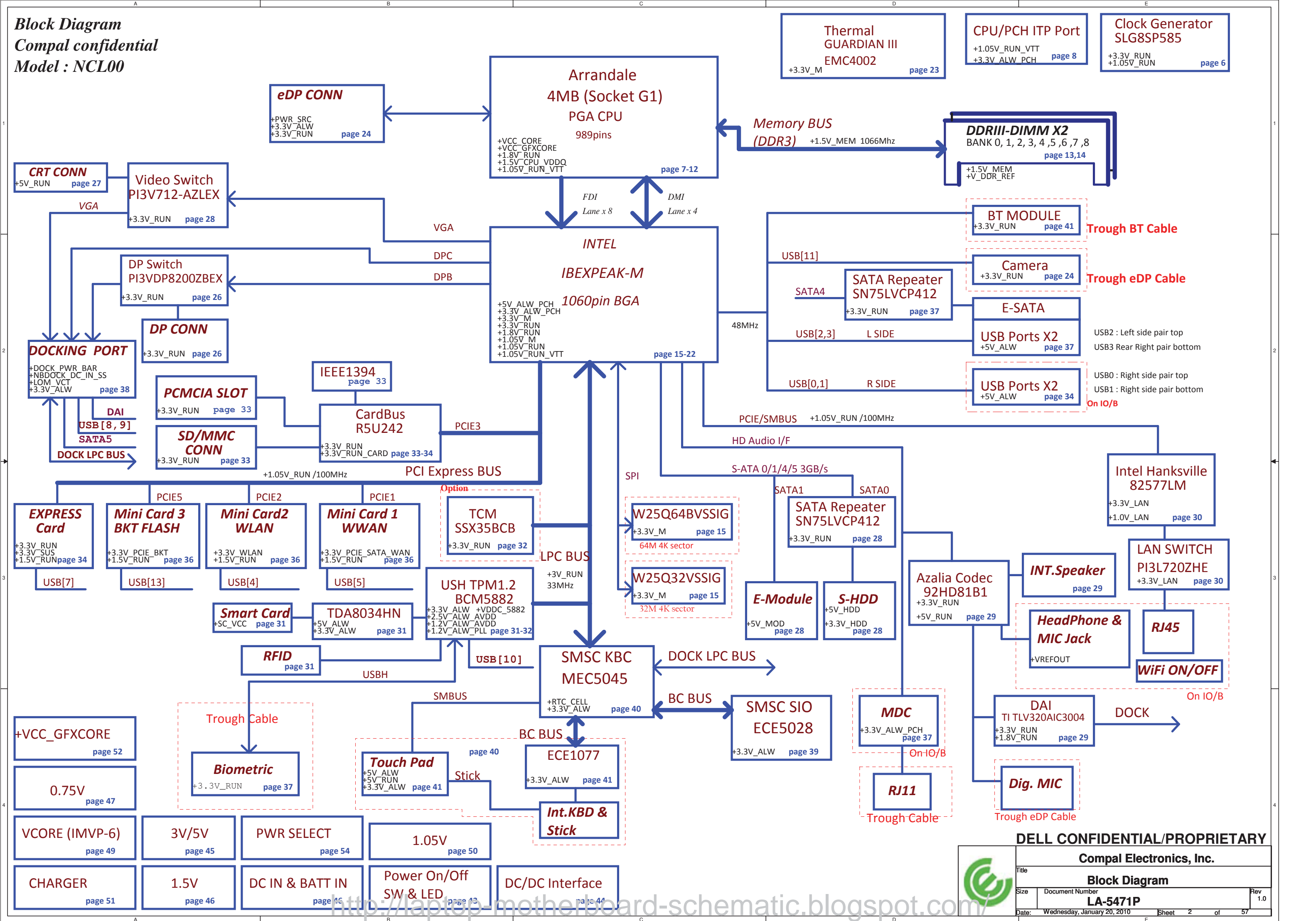
MB PCB	
Part Number	Description
DA80000G700	PCB 0AY LA-5471P REV0 M/B UMA

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***Block Diagram***  
***Compal confidential***  
***Model : NCL00***



POWER STATES

Signal State	SLP S3#	SLP S4#	SLP S5#	S4 STATE#	SLP M#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M1	LOW	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M1	LOW	LOW	HIGH	LOW	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M1	LOW	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

power plane State	+15V_ALW +5V_ALW +3.3V_ALW_PCH +3.3V_RTC_LDO	+3.3V_SUS +1.5V_MEM	+5V_RUN +3.3V_RUN +1.8V_RUN +1.5V_RUN +0.75V_DDR_VTT +VCC_CORE +1.05V_RUN_VTT +1.05V_RUN	+3.3V_M +1.05V_M	+3.3V_M +1.05V_M (M-OFF)
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF
S5 S4/AC don't exist	OFF	OFF	OFF	OFF	OFF

PCH	USB PORT#	DESTINATION
	0	JUSB1 (Ext Right Side Top)
	1	JUSB1 (Ext Right Side Bottom)
	2	JESA1 (Ext Left Side Top)
	3	JESA1 (Ext Left Side Bottom)
	4	WLAN
	5	WWAN
	6	Bluetooth
	7	USH->BIO
	8	DOCKING
	9	DOCKING
	10	Express card
	11	Camera
	12	none
	13	JMINI3(PCIE/BKT CARD)

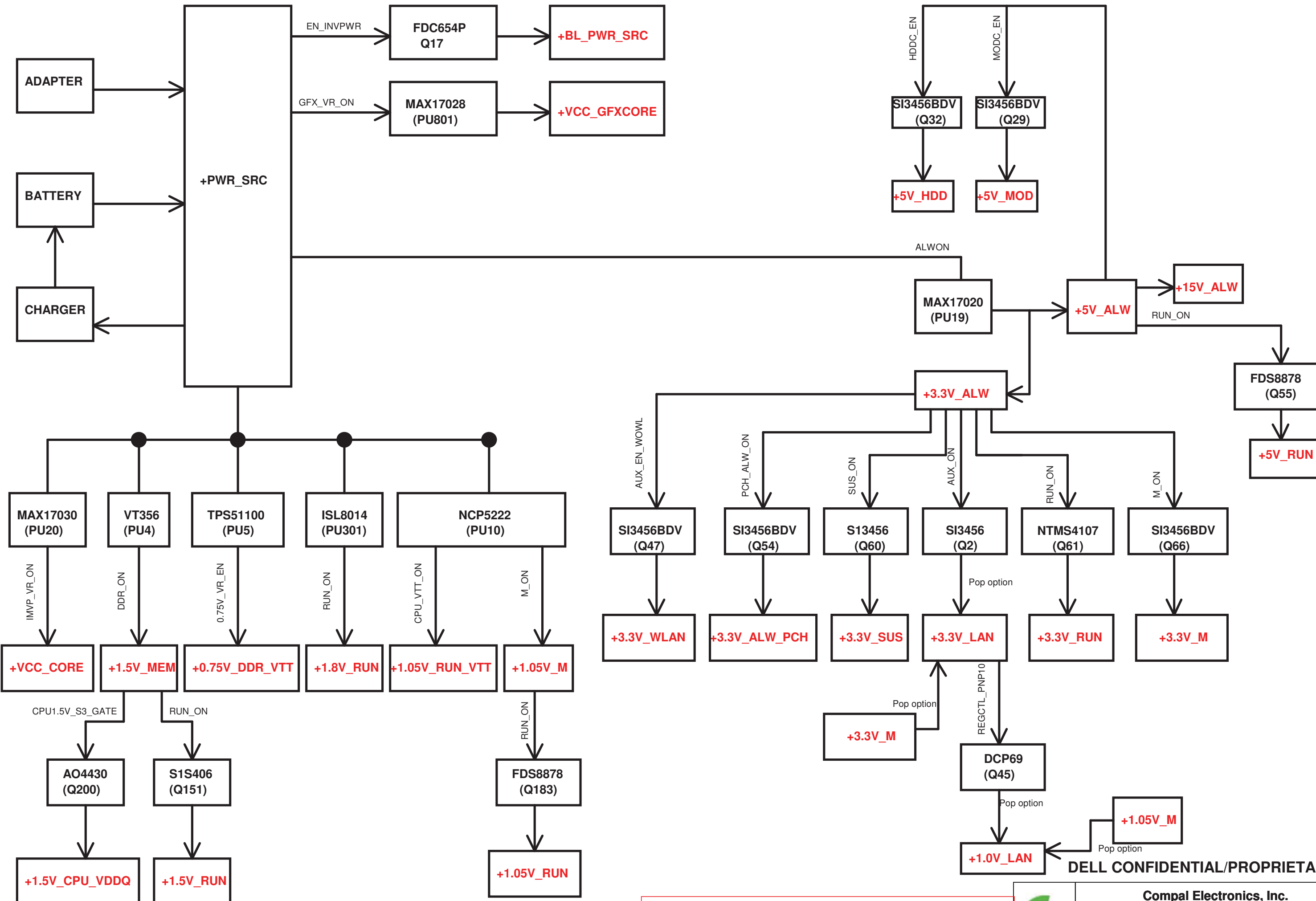
PCI EXPRESS	DESTINATION
Lane 1	MINI CARD-1 WWAN
Lane 2	MINI CARD-2 WLAN
Lane 3	PCMCIA
Lane 4	EXPRESS CARD
Lane 5	MINI CARD-3 PCIE/BKT
Lane 6	10/100/1G LAN
Lane 7	None
Lane 8	None

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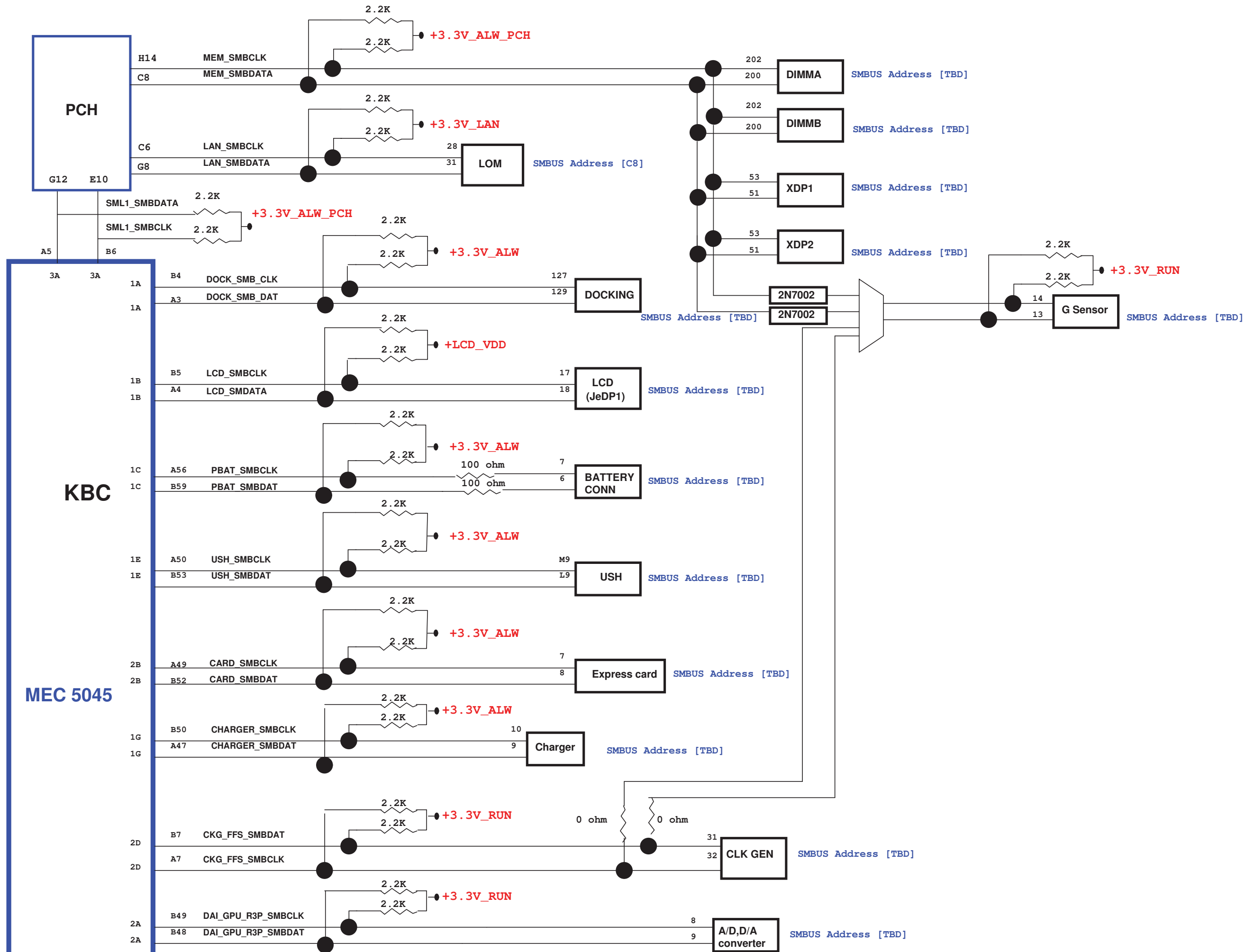


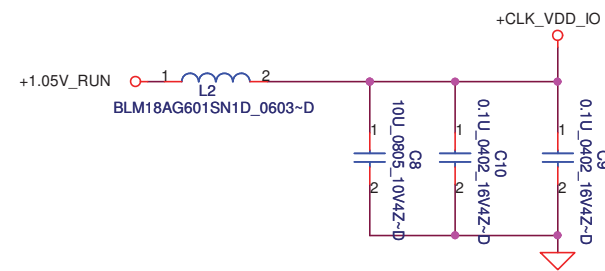
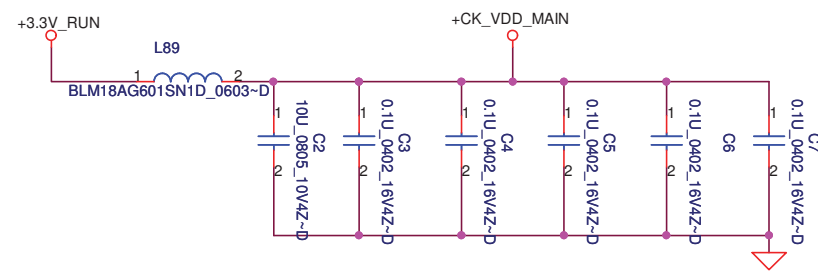
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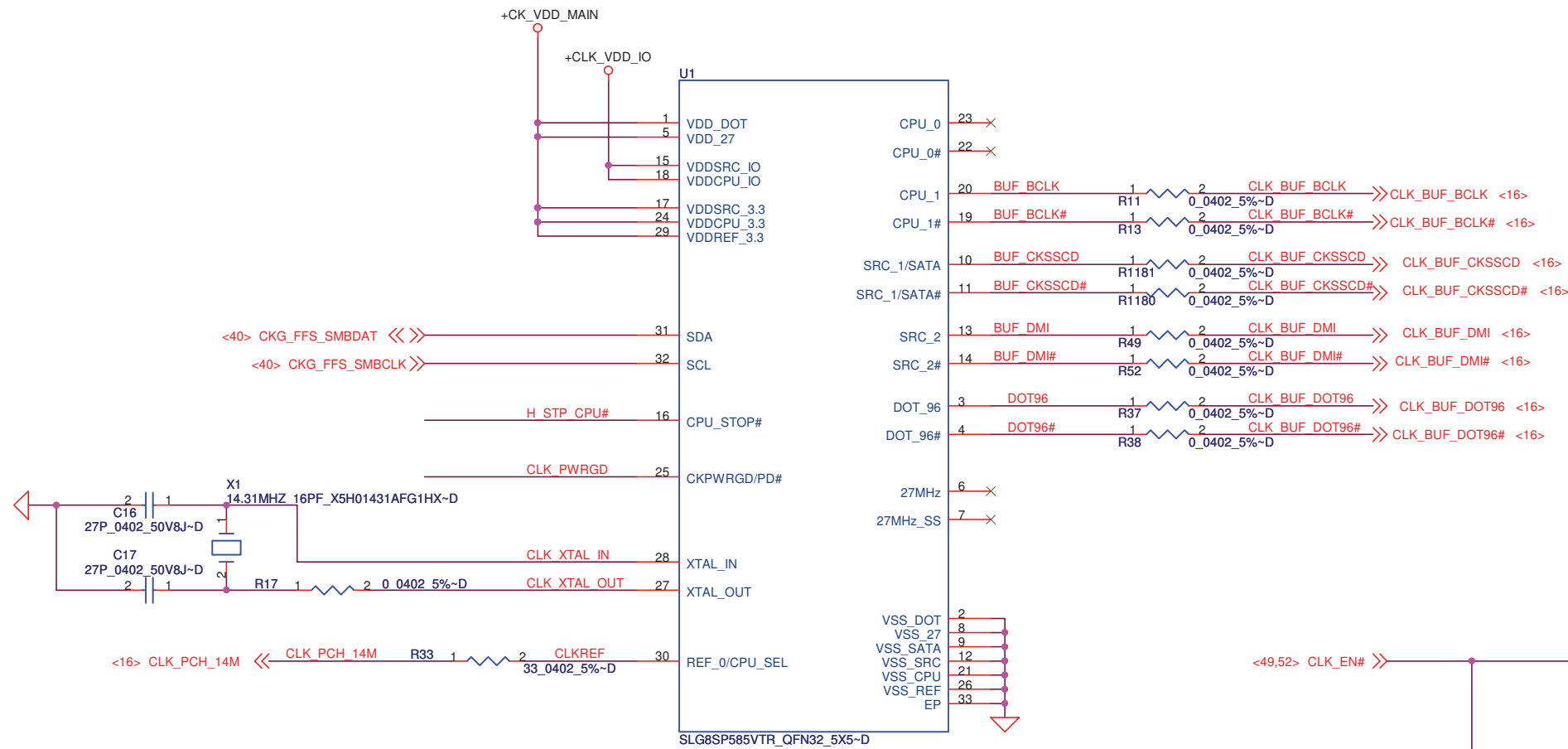
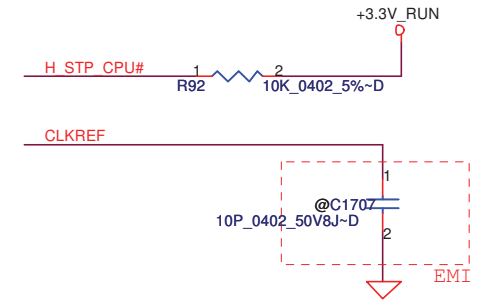


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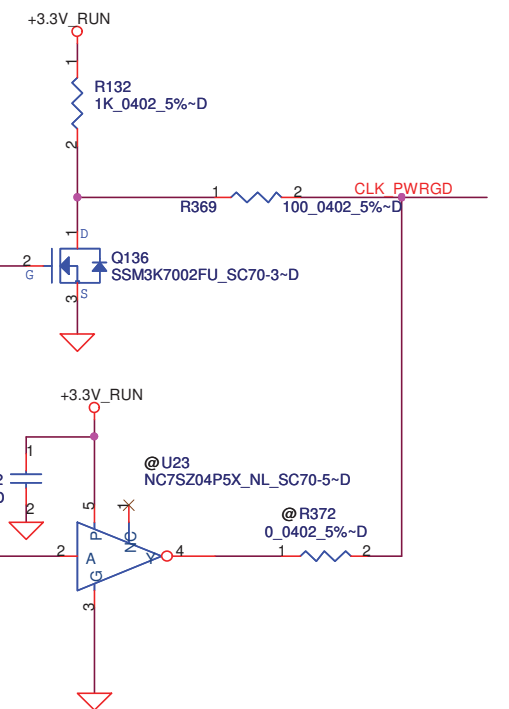
+CLK\_VDD\_IO CAN BE CHANGE FROM 1.05V TO 3V



change PN to Spectra Linear SL28748ELCT SA00002Y33L

REF\_0/CPU\_SEL

PIN 30	CPU0	CPU1
1 (0.7~1.5v)	100MHz	100MHz
0 (DEFAULT)	133MHz	133MHz



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Clock Generator

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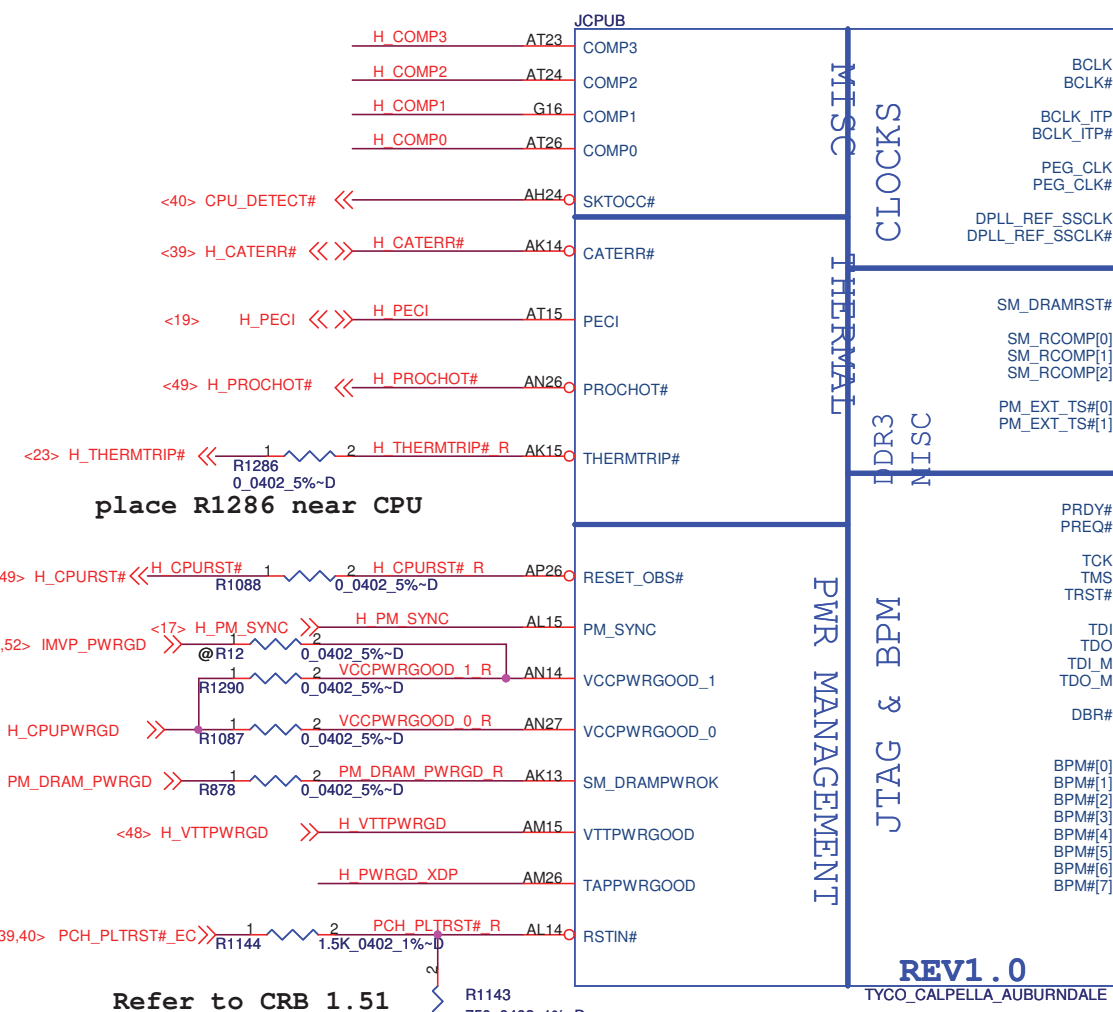
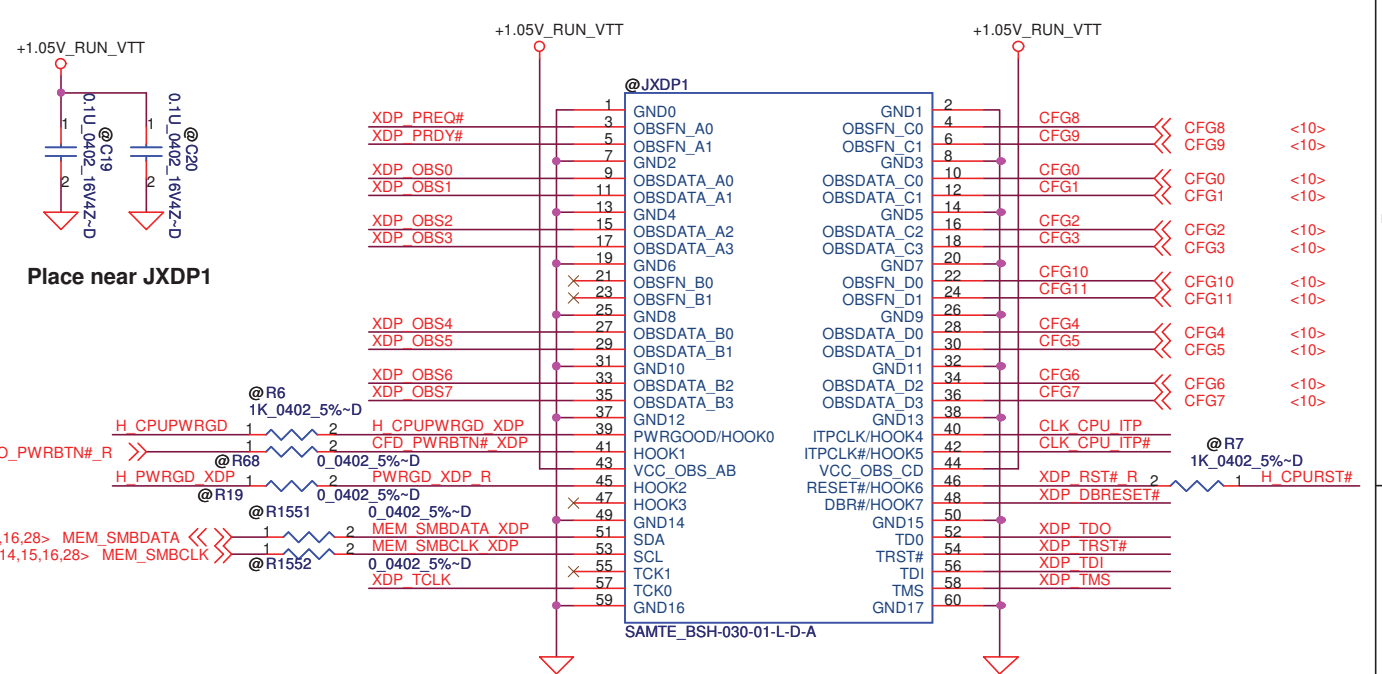
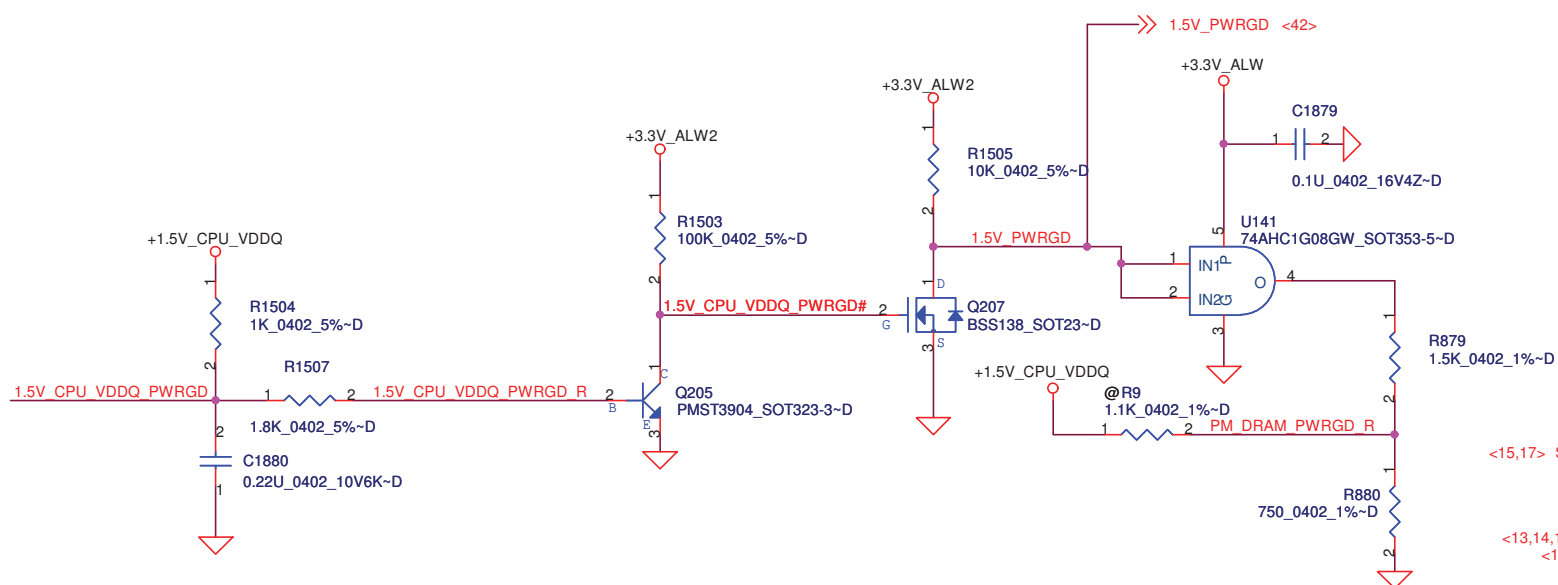
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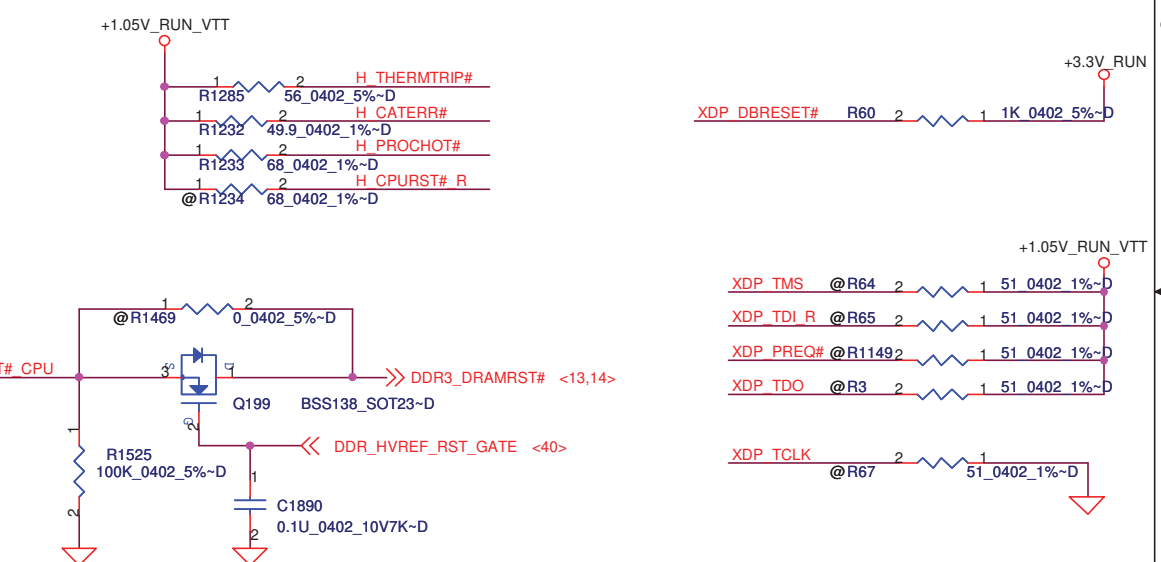
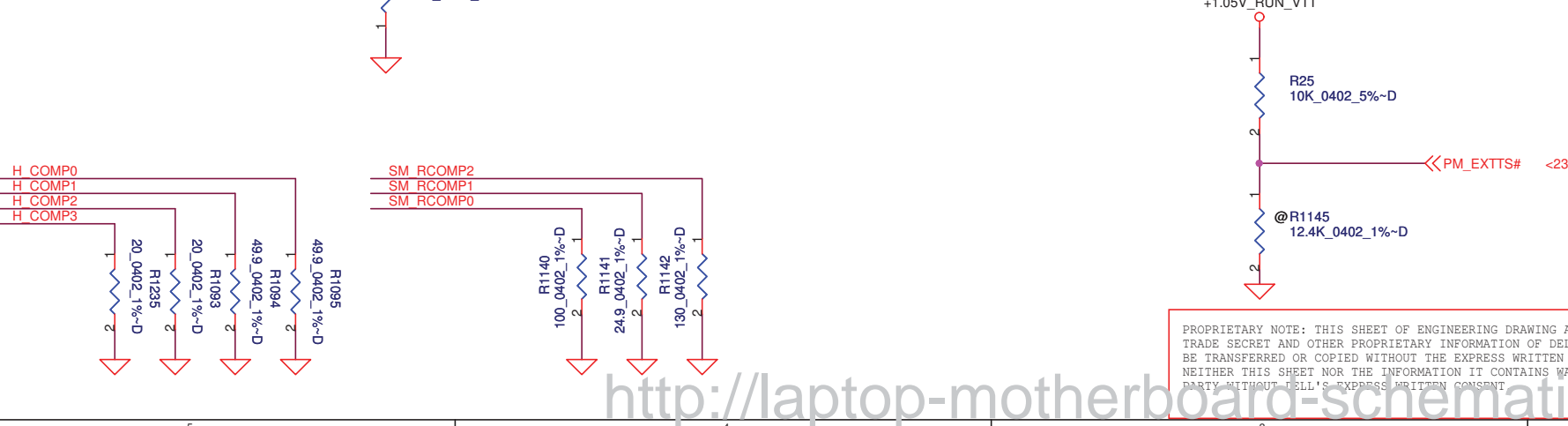
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Keep R1132, R1133, R1136-R119 for slew rate control.



### JTAG MAPPING

Signal	Pin	Value
XDP_TDI_R	@R1153	0.0402 5%-D
XDP_TDI_M	@R1155	0.0402 5%-D
XDP_TDI	@R1154	0.0402 5%-D
XDP_TDO_M	@R1154	0.0402 5%-D
XDP_TDO_R	@R1156	0.0402 5%-D
XDP_TDO	@R1153	0.0402 5%-D
XDP_TRST#	@R66	51.0402 1%-D

Scan Chain	Stuff ->
(Default)	Stuff -> R1153,R1156,R1157
	No stuff -> R1154,R1155
CPU Only	Stuff -> R1153,R1154
	No stuff -> R1154,R1155,R1157
PCH Only	Stuff -> R1155,R1156
	No stuff -> R1153,R1154,R1157

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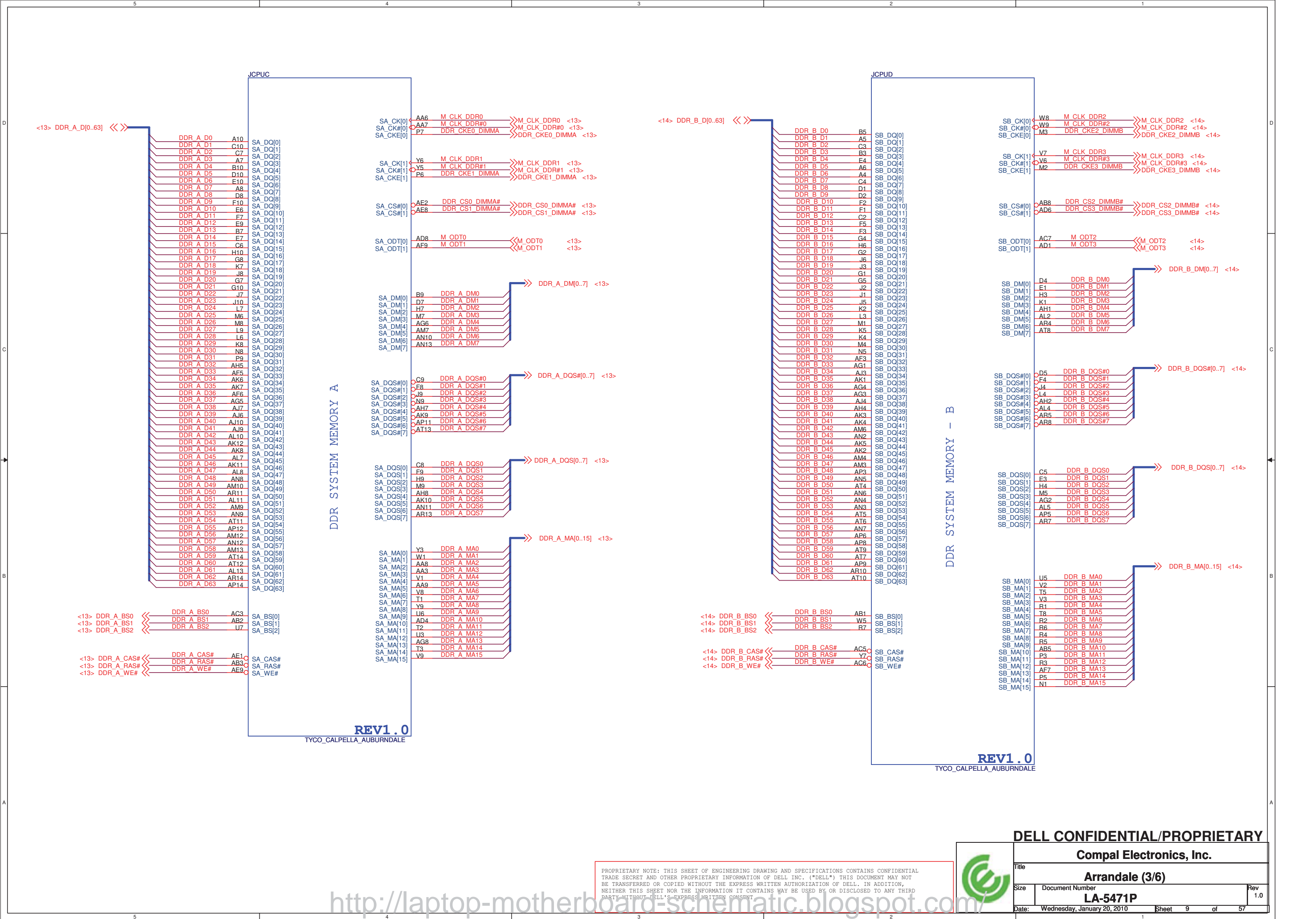
**Arrandale (2/6)**

**LA-5471P**

Rev 1.0

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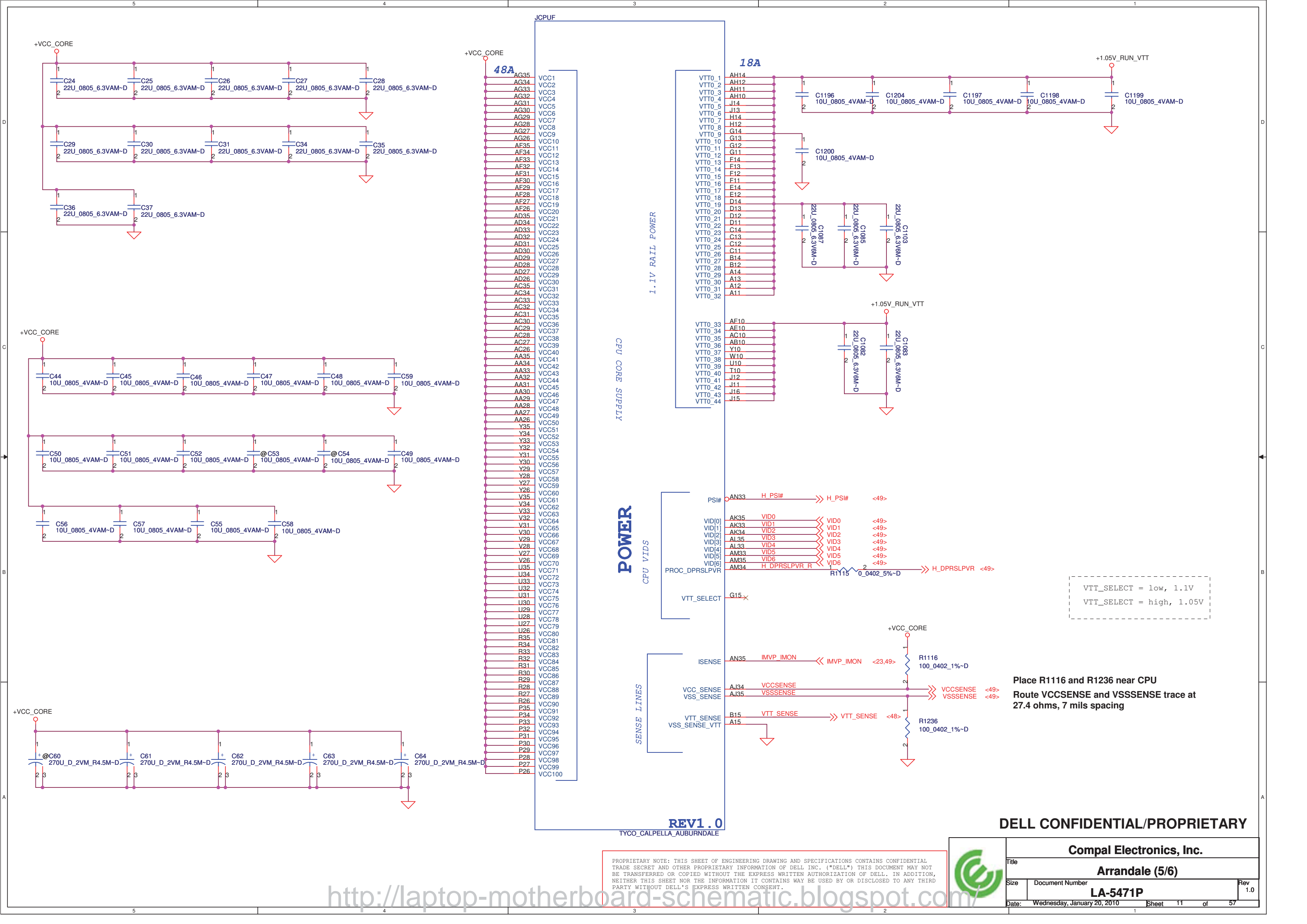
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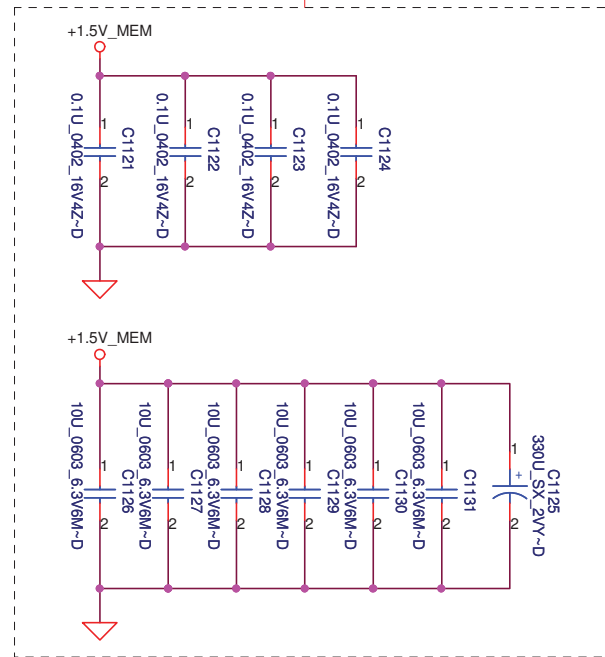




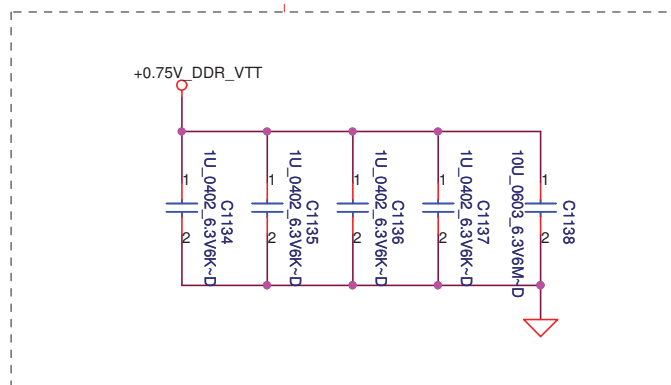


<9> DDR\_A\_DQS#[0..7] <<>>  
<9> DDR\_A\_D[0..63] <<>>  
<9> DDR\_A\_DM[0..7] <<>>  
<9> DDR\_A\_DQS[0..7] <<>>  
<9> DDR\_A\_MA[0..15] <<>>

Layout Note:  
Place near JDIMMA

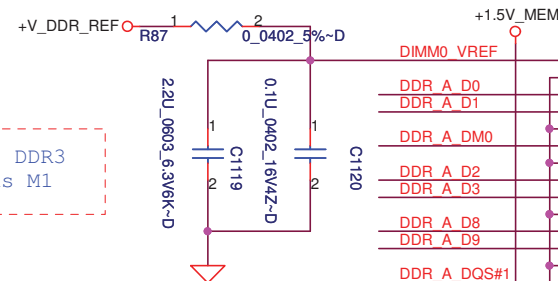


Layout Note:  
Place near JDIMMA.203,204



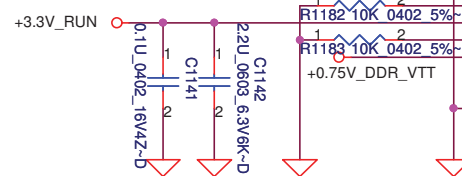
Populate R87 for Intel DDR3  
VREFDQ multiple methods M1

Note:  
Check voltage tolerance of  
VREF\_DQ at the DIMM socket



<9> DDR\_CKE0\_DIMMA <<>> DDR CKE0 DIMMA  
<9> DDR\_A\_BS2 <<>> DDR A BS2  
DDR A MA12  
DDR A MA9  
DDR A MA8  
DDR A MA5  
DDR A MA3  
DDR A MA1  
M CLK DDR0  
M CLK DDR#0  
DDR A MA10  
DDR A BS0  
DDR A WE#  
DDR A CAS#  
DDR A MA13  
DDR CS1 DIMMA#

DDR A D32  
DDR A D33  
DDR A DQS#4  
DDR A DQS4  
DDR A D34  
DDR A D35  
DDR A D40  
DDR A D41  
DDR A DM5  
DDR A D42  
DDR A D43  
DDR A D48  
DDR A D49  
DDR A DQS#6  
DDR A DQS6  
DDR A D50  
DDR A D51  
DDR A D56  
DDR A D57  
DDR A DM7  
DDR A D58  
DDR A D59



JDIMMA  
VREF\_DQ  
VSS  
DQ4  
DQ0  
DQ1  
DQ5  
DQ10  
DQ11  
DQ15  
DQ16  
DQ17  
DQ20  
DQ21  
DQ22  
DQ23  
DQ24  
DQ25  
DQ26  
DQ27  
VSS  
CKE0  
VDD  
NC  
BA2  
VDD  
A12/BC#  
A9  
VDD  
A8  
A6  
A4  
VDD  
A2  
A0  
VDD  
CK1  
CK0  
CK1#  
VDD  
BA1  
RAS#  
VDD  
S0#  
ODT0  
VDD  
ODT1  
NC  
VDD  
TEST  
CA  
VSS  
DQ36  
DQ37  
VSS  
DM4  
VSS  
DQ38  
DQ39  
DQ40  
DQ41  
VSS  
DM5  
VSS  
DQ42  
DQ43  
VSS  
DQ44  
DQ45  
VSS  
DQ46  
DQ47  
VSS  
DQ48  
DQ49  
VSS  
DQ50  
DQ51  
VSS  
DQ52  
DQ53  
VSS  
DM6  
VSS  
DQ54  
DQ55  
VSS  
DQ56  
DQ57  
VSS  
DM7  
VSS  
DQ58  
DQ59  
VSS  
SA0  
VDDSPD  
SDA  
SCL  
VTT  
GND1  
FOX\_AS0A626-U4SN-7F

DDR CKE1 DIMMA <<>> DDR\_CKE1\_DIMMA <9>  
DDR A MA15  
DDR A MA14  
DDR A MA11  
DDR A MA7  
DDR A MA6  
DDR A MA4  
DDR A MA2  
DDR A MA0  
M CLK DDR1  
M CLK DDR#1  
M CLK DDR#1 <9>  
DDR A BS1  
DDR A RAS#  
DDR CS0 DIMMA#  
M ODT0  
M ODT1

DDR A D36  
DDR A D37  
DDR A DM4  
DDR A D38  
DDR A D39  
DDR A D44  
DDR A D45  
DDR A DQS#5  
DDR A DQS5  
DDR A D46  
DDR A D47  
DDR A D52  
DDR A D53  
DDR A DM6  
DDR A D54  
DDR A D55  
DDR A D60  
DDR A D61  
DDR A DQS#7  
DDR A DQS7  
DDR A D62  
DDR A D63  
MEM SMBDATA <<>> MEM\_SMBDATA <8,14,15,16,28>  
MEM SMBCLK <<>> MEM\_SMBCLK <8,14,15,16,28>  
+0.75V\_DDR\_VTT



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DDRIII-SODIMM SLOT1

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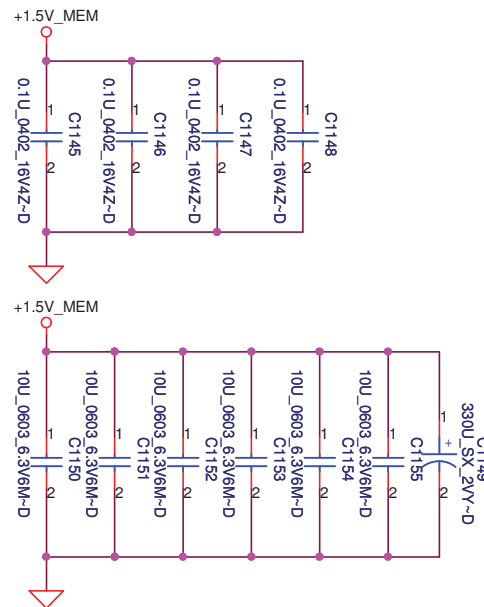


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<9> DDR\_B\_D[0..63] <<>>  
<9> DDR\_B\_DM[0..7] <<>>  
<9> DDR\_B\_DQS[0..7] <<>>  
<9> DDR\_B\_MA[0..15] <<>>

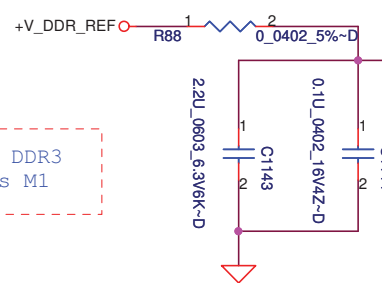
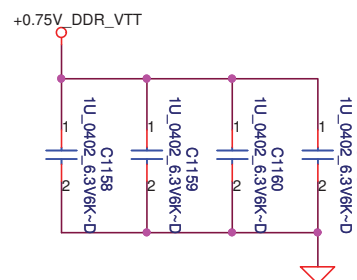
Populate R88 for Intel DDR3  
VREFDQ multiple methods M1

Note:  
Check voltage tolerance of  
VREF\_DQ at the DIMM socket

Layout Note:  
Place near JDIMMB

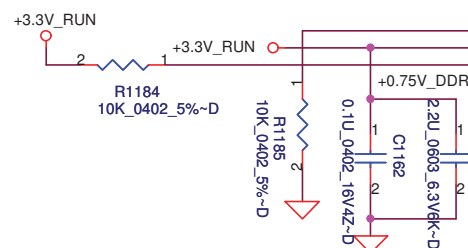


Layout Note:  
Place near JDIMMB.203,204



<9> DDR\_CKE2\_DIMMB >> DDR CKE2 DIMMB  
<9> DDR\_B\_BS2 >> DDR B BS2  
<9> M\_CLK\_DDR2 >> M\_CLK\_DDR2  
<9> M\_CLK\_DDR#2 >> M\_CLK\_DDR#2  
<9> DDR\_B\_BS0 >> DDR B BS0  
<9> DDR\_B\_WE# >> DDR B WE#  
<9> DDR\_B\_CAS# >> DDR B CAS#  
<9> DDR\_CS3\_DIMMB# >> DDR CS3 DIMMB#

DDR B D32  
DDR B D33  
DDR B D34  
DDR B D35  
DDR B D40  
DDR B D41  
DDR B D42  
DDR B D43  
DDR B D48  
DDR B D49  
DDR B D50  
DDR B D51  
DDR B D56  
DDR B D57  
DDR B D58  
DDR B D59



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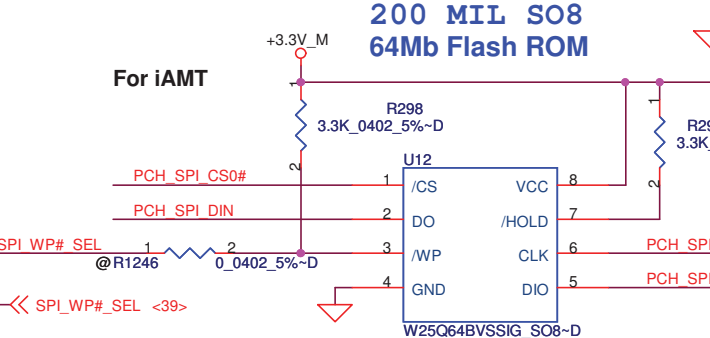
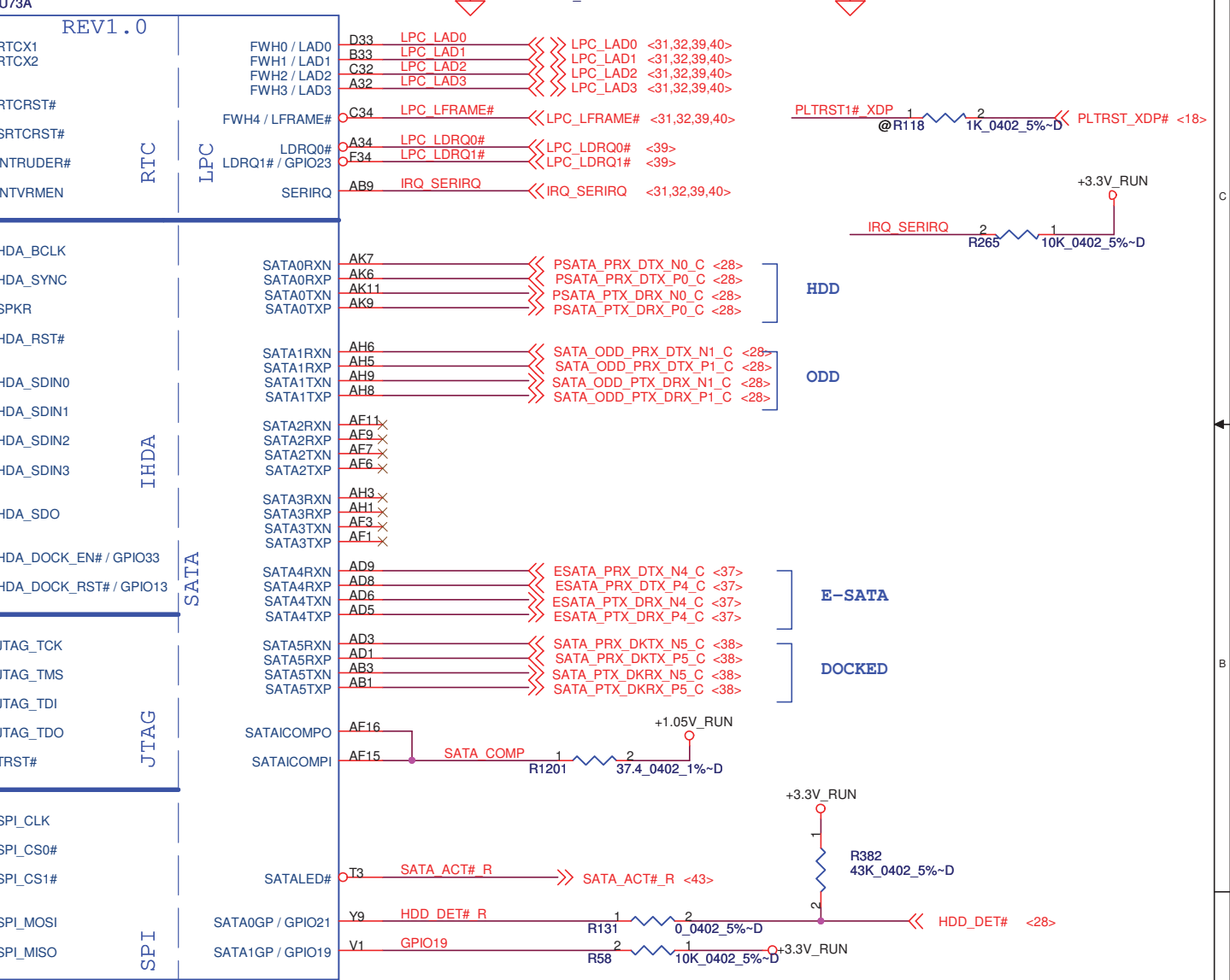
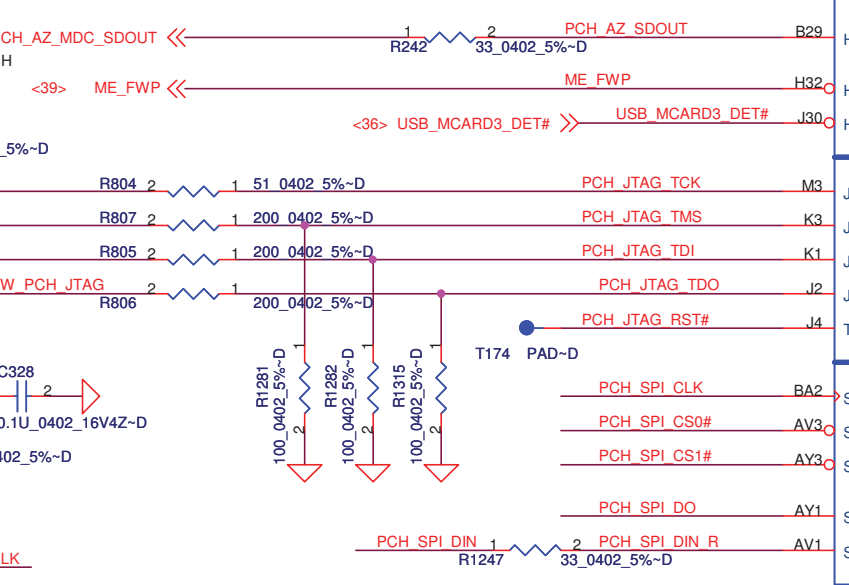
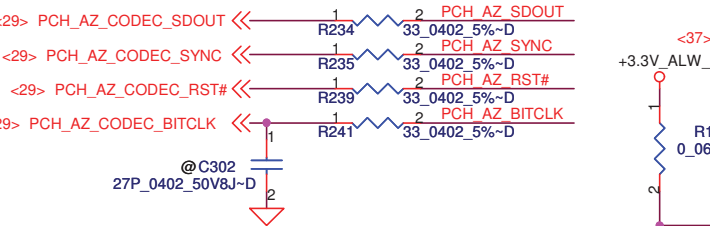
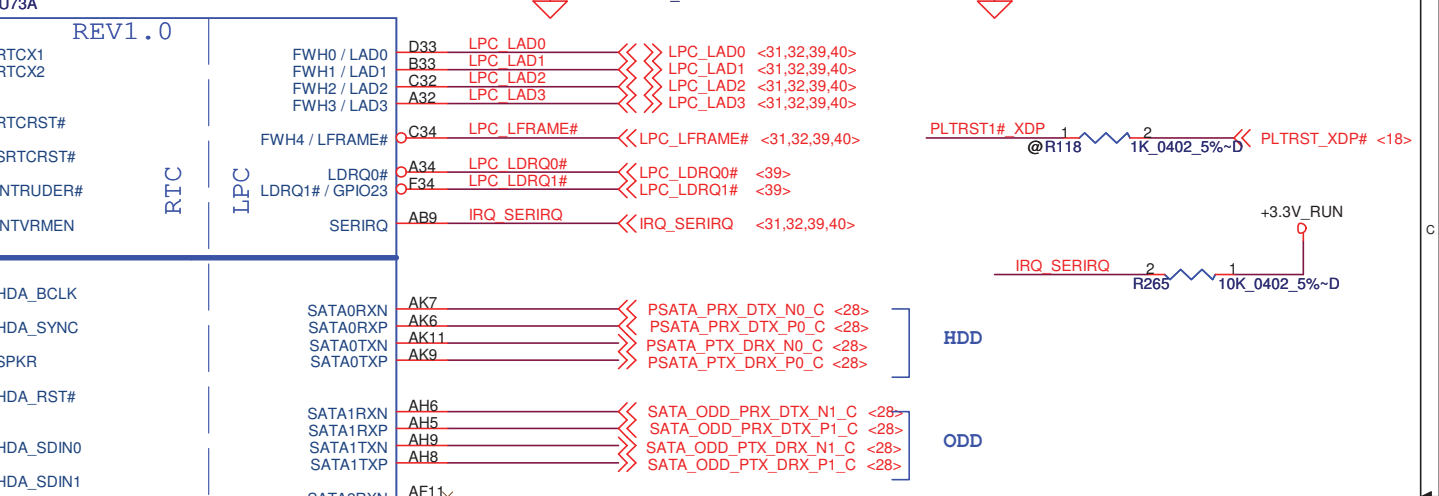
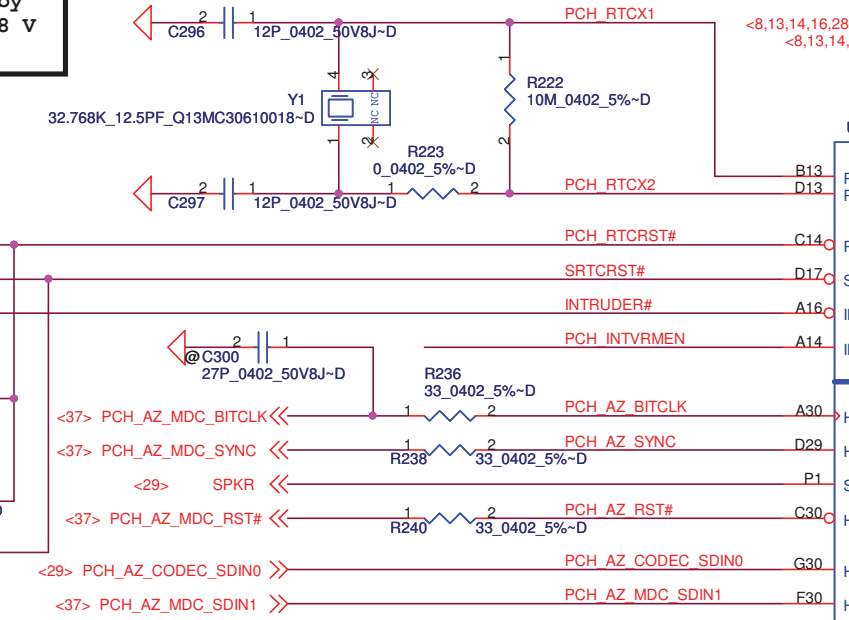
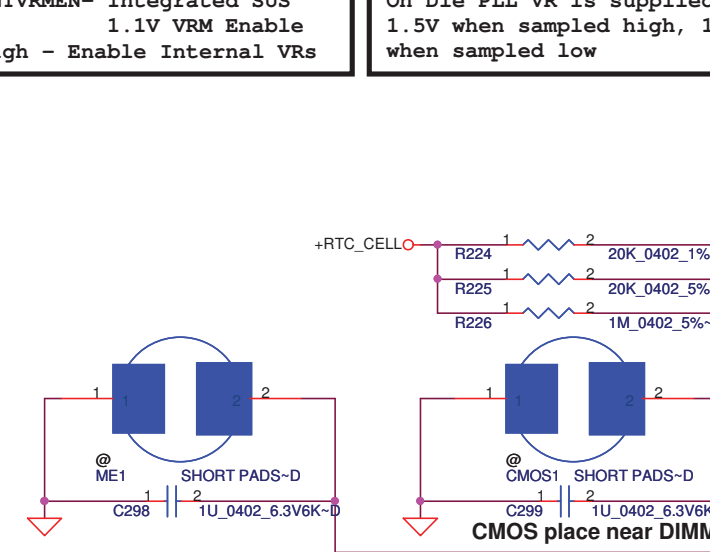
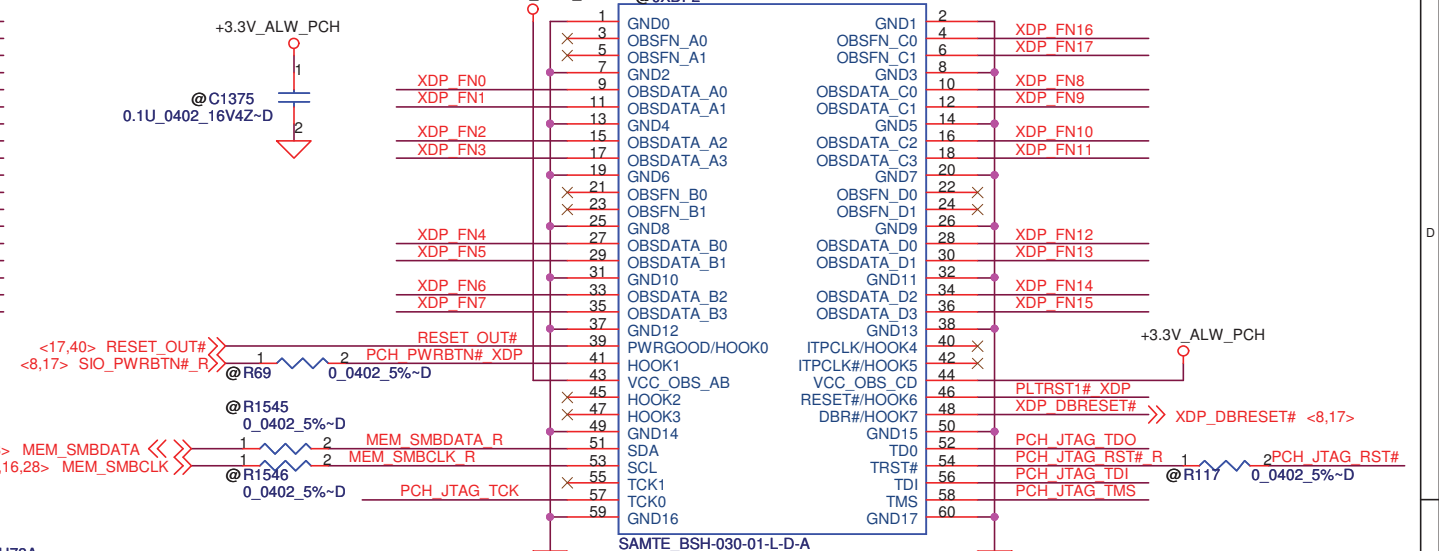
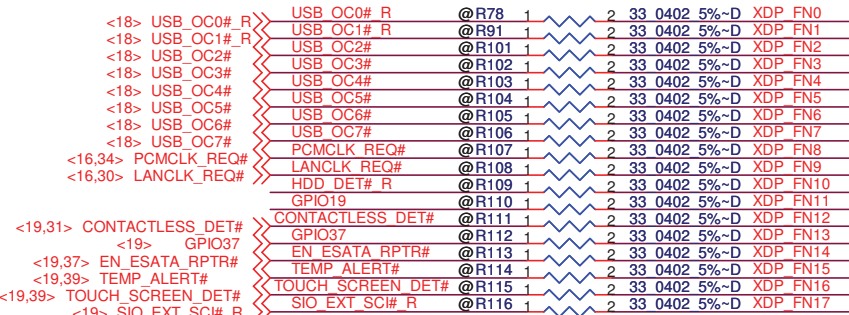
DDRIII-SODIMM SLOT2

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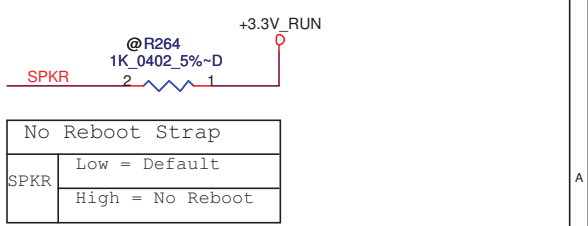
ME_CLR1	TPM setting
Shunt	Clear ME RTC Registers
Open	Keep ME RTC Registers



On Die PLL VR is supplied by 1.5V when sampled high, 1.8 V when sampled low



		PCH JTAG Enable		PCH JTAG Disable		Production
PCH Pin	Ref.	ES1	ES2	ES1	ES2	*All
TDO	R806	No Stuff	200 ohm	No Stuff	No Stuff	200 ohm
	R1315	No Stuff	100 ohm	No Stuff	No Stuff	100 ohm
TMS	R807	200 ohm	200 ohm	No Stuff	No Stuff	200 ohm
	R1281	100 ohm	100 ohm	No Stuff	No Stuff	100 ohm
TDI	R805	200 ohm	200 ohm	20K ohm	No Stuff	200 ohm
	R1282	100 ohm	100 ohm	10K ohm	No Stuff	100 ohm
TCK	R804	4.7K ohm	4.7K ohm	4.7K ohm	4.7K ohm	51 ohm
TRST#	R808	20K ohm	No Stuff	No Stuff	No Stuff	No Stuff
	R1316	10K ohm	No Stuff	No Stuff	No Stuff	No Stuff



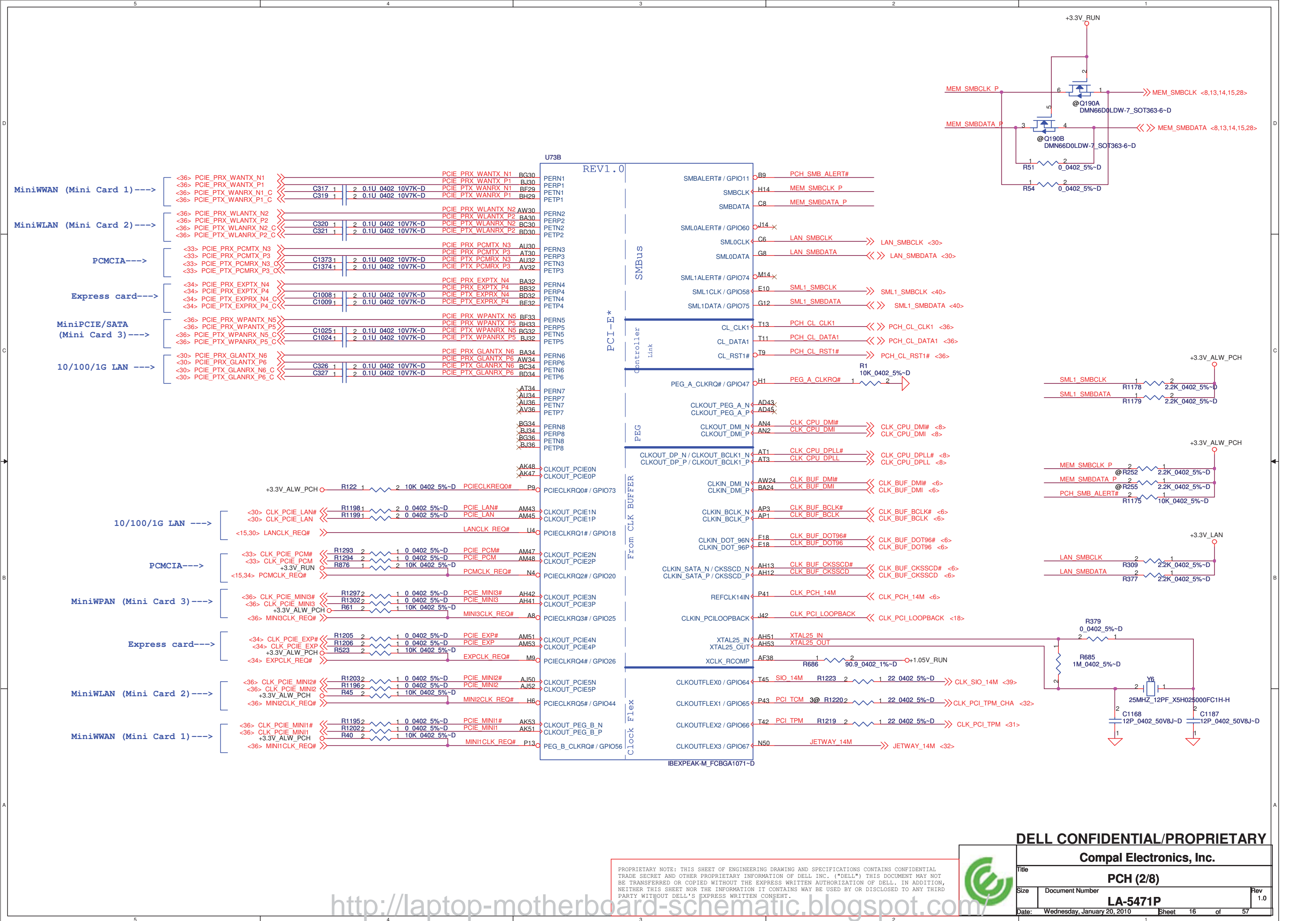
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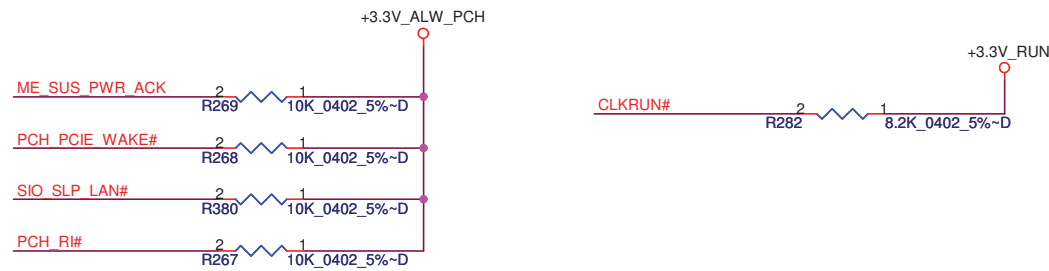
**PCH (1/8)**

**LA-5471P**

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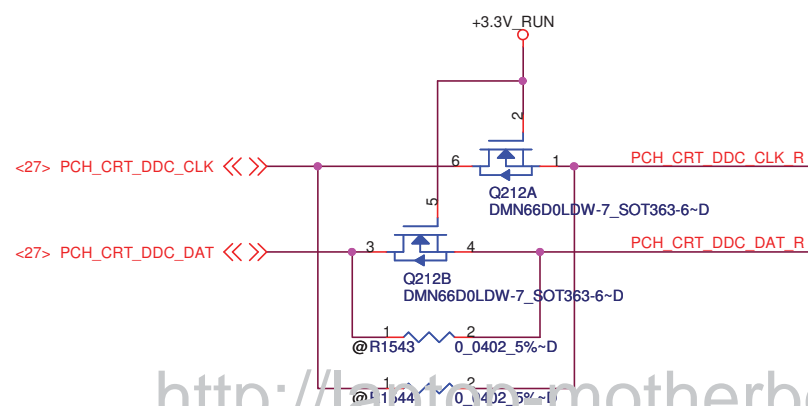
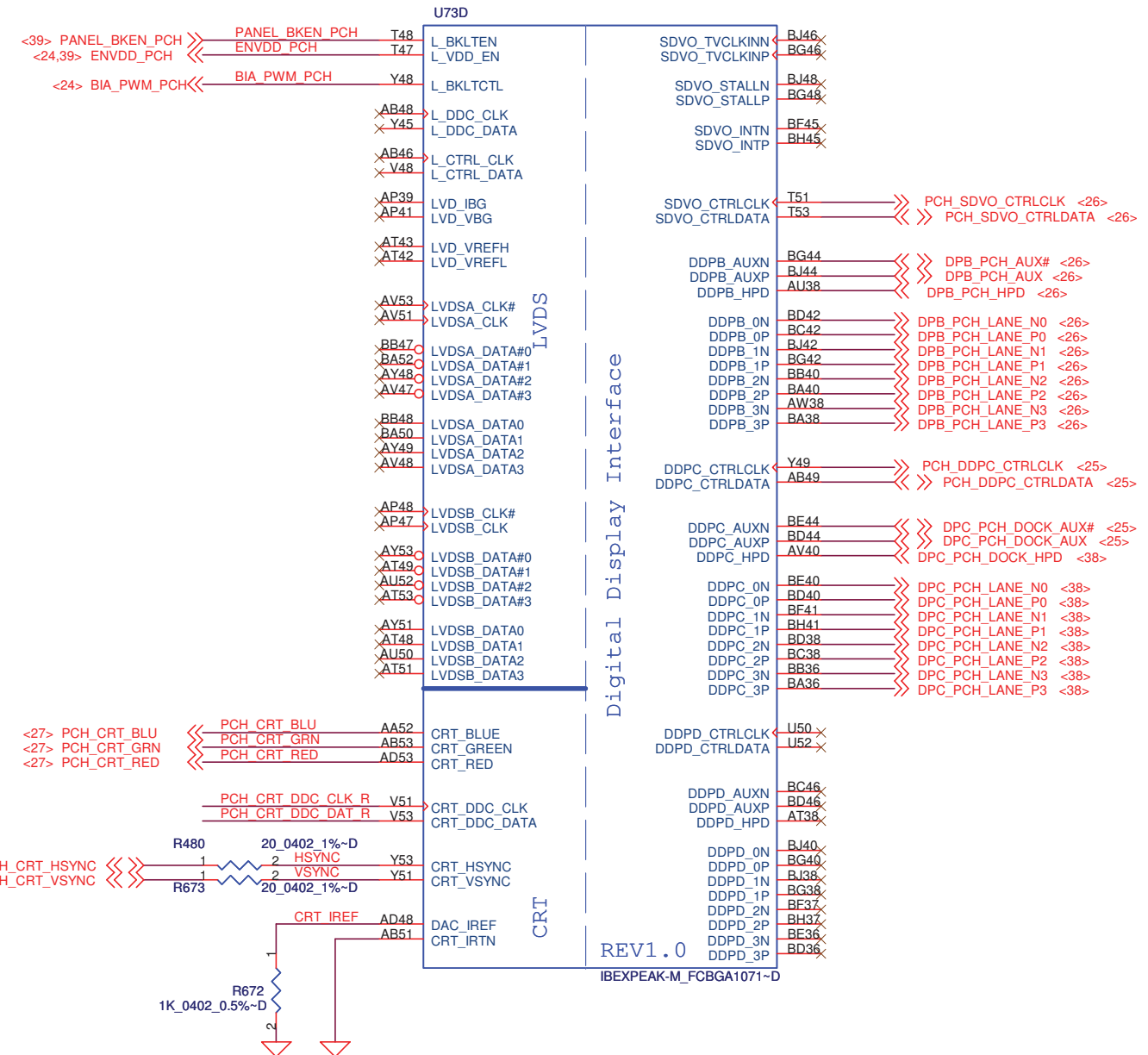
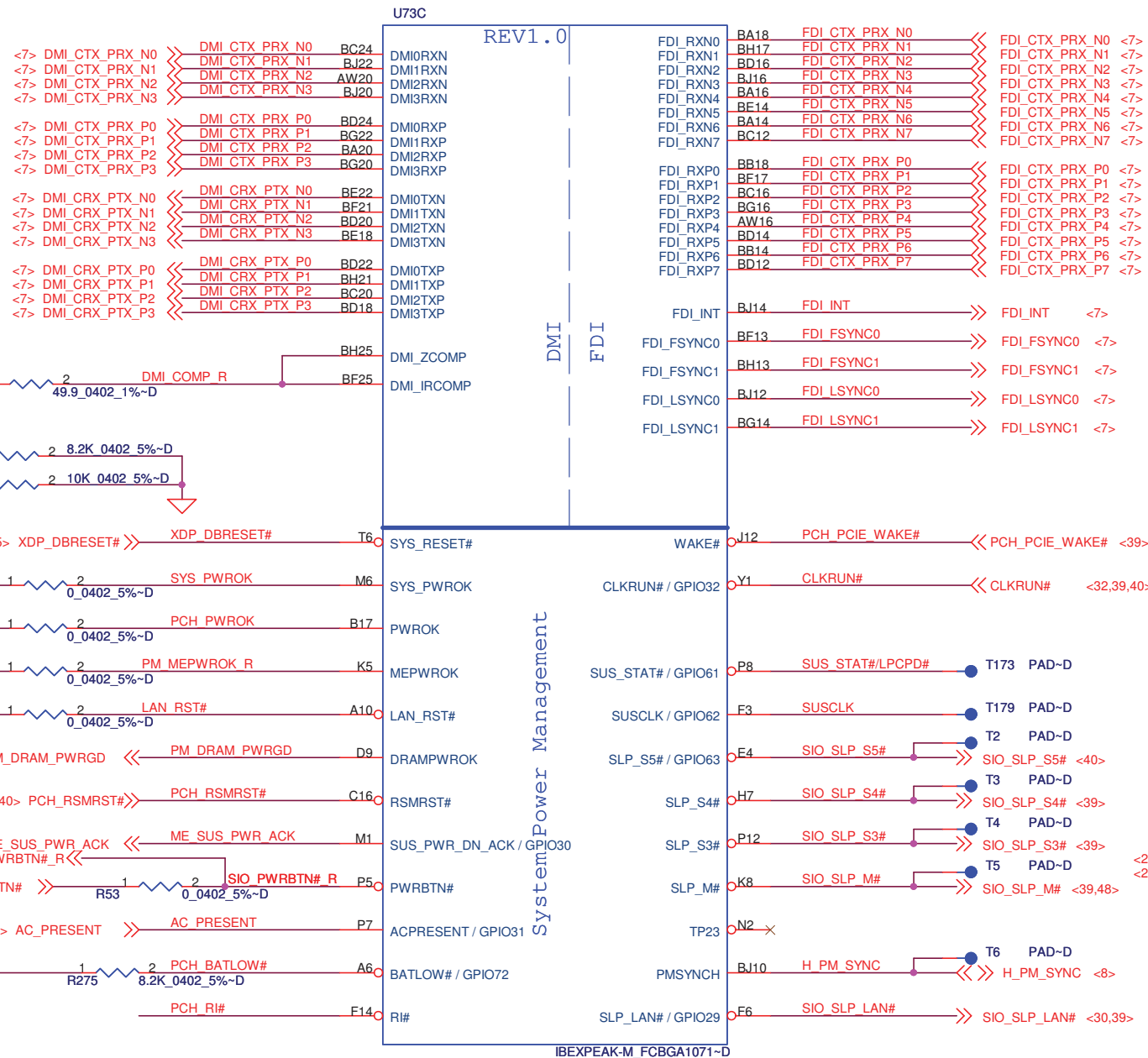




#### Intel WW18 Strapping option

PORT	STRAP	ENABLE	DISABLE
LVDS	L_DDC_DATA	PU to 3.3V thooough 2.2Kohm	NC
PORT B	SDVO_CTRLDATA	PU to 3.3V thooough 2.2Kohm	NC
PORT B	DDPC_CTRLDATA	PU to 3.3V thooough 2.2Kohm	NC
PORT B	DDPD_CTRLDATA	PU to 3.3V thooough 2.2Kohm	NC
eDP on CPU	CFG[4] (at CPU)	PD to GND thooough 3.3Kohm	NC

#### Intel request DDPB can not support eDP



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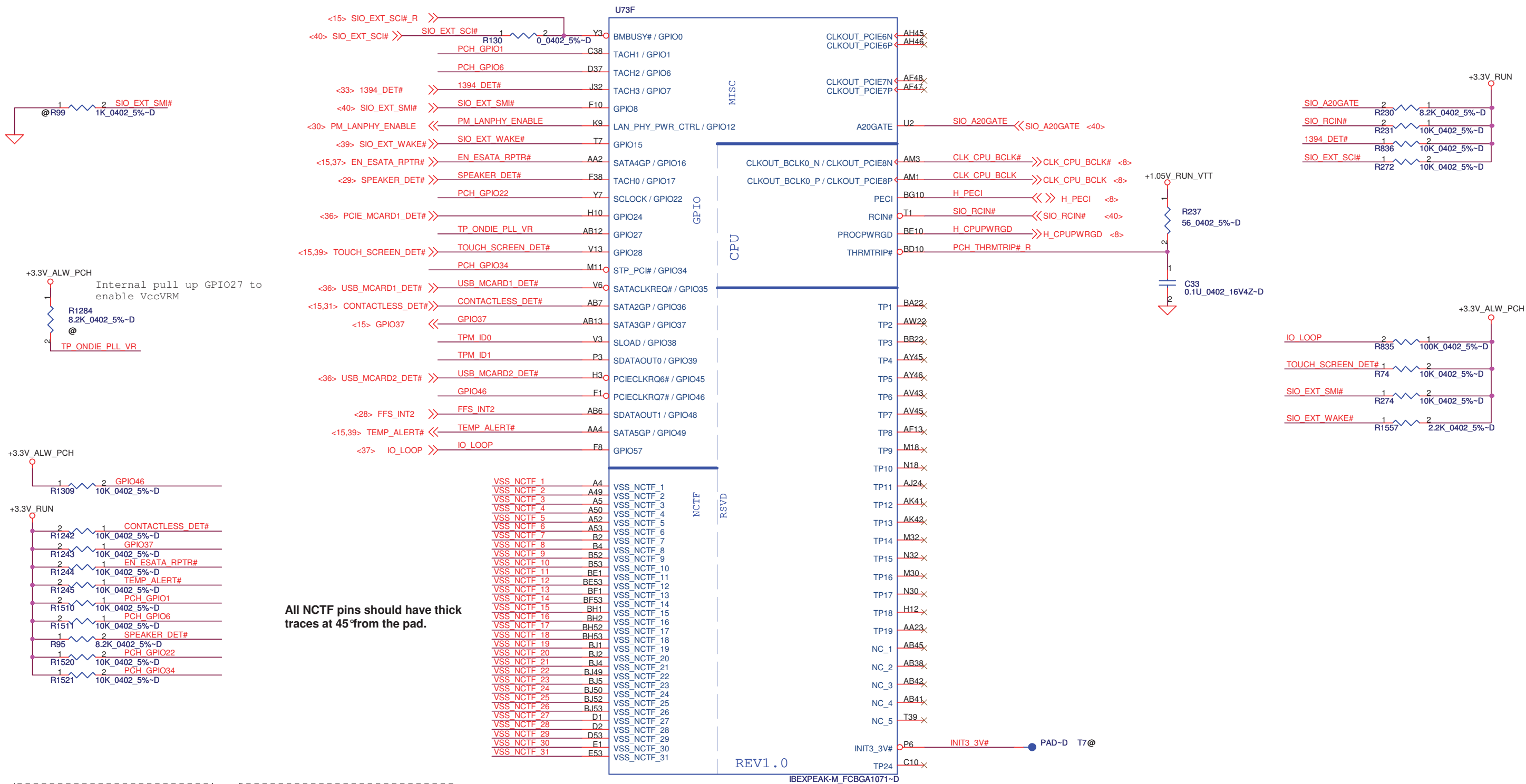


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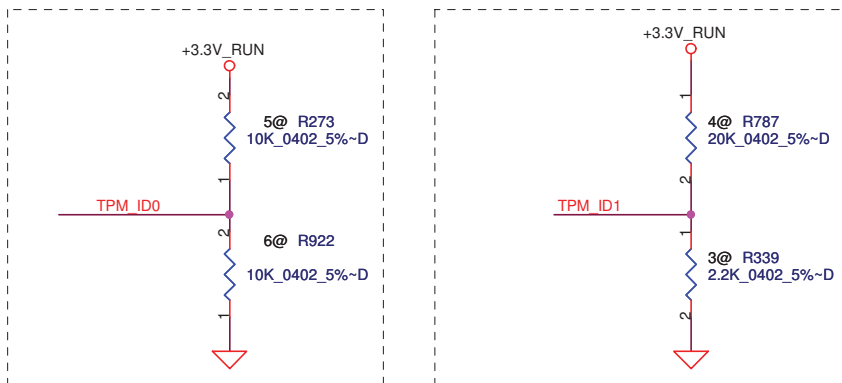
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All NCTF pins should have thick traces at 45° from the pad.



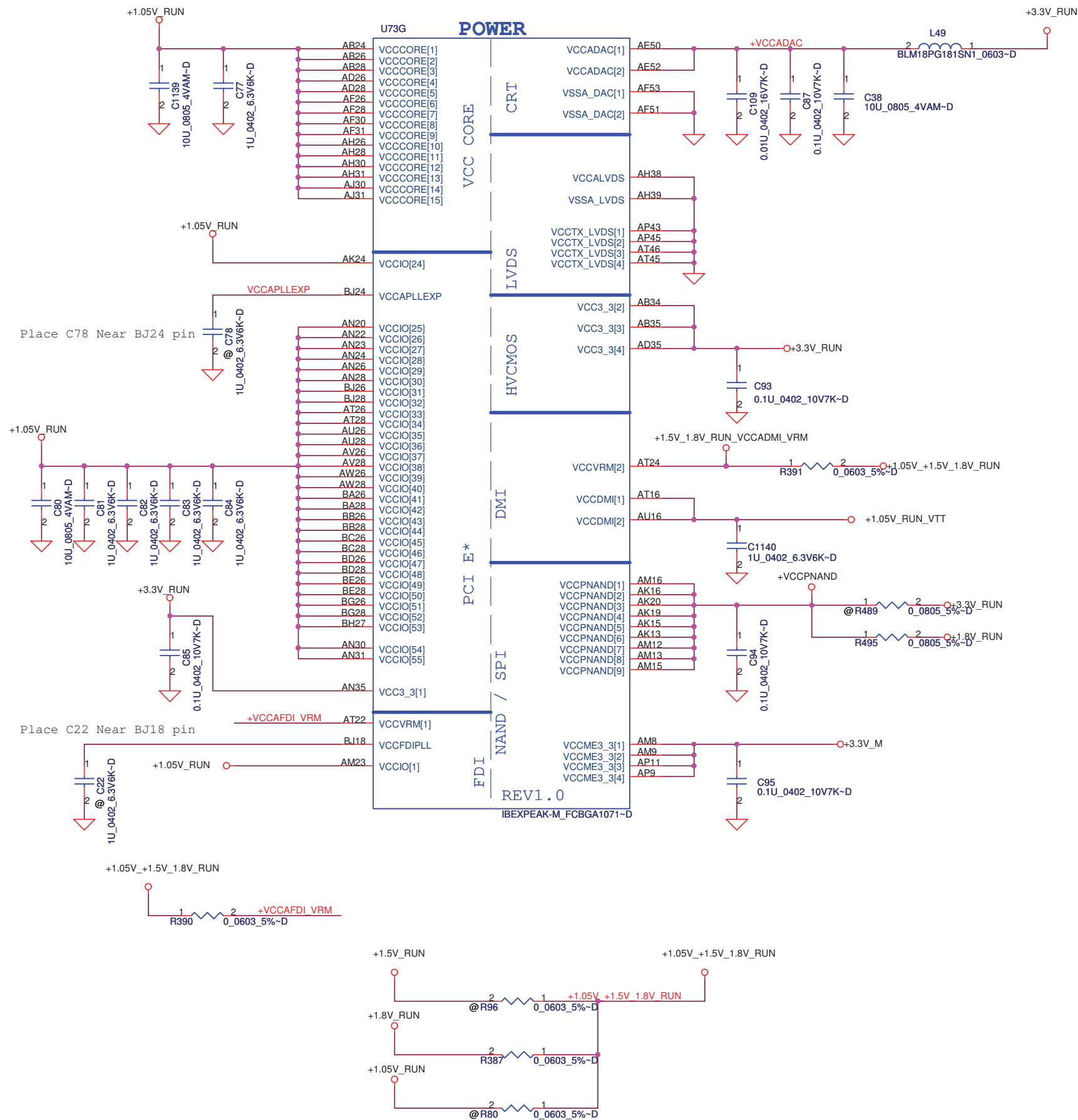
	TPM_ID0	TPM_ID1
China TPM	0	0
No TPM, No China TPM	0	1
Reserved	1	0
TPM	1	1

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PCH Power Rail Table		
Voltage Rail	Voltage	S0 Iccmax Current (A)
V_CPU_IO	1.1/1.05	< 1 (mA)
V5REF	5	< 1 (mA)
V5REF_Sus	5	< 1 (mA)
Vcc3_3	3.3	0.357
VccAClk	1.1	0.052
VccADAC	3.3	0.069
VccADPLLA	1.1	0.068
VccADPLLB	1.1	0.069
Vccap11EXP	1.1	0.04
VccCore	1.1	1.432
VccDMI	1.1	0.058
VccDMI	1.1	0.061
VccFDIPLL	1.1	0.037
VccIO	1.1	3.062
VccLAN	1.1	0.32
VccME	1.1	1.849
VccME3_3	3.3	0.085
VccpNAND	1.8	0.156
VccRTC	3.3	2 (mA)
VccSATAPLL	1.1	0.031
VccSus3_3	3.3	0.163
VccSusHDA	3.3	0.006
VccVRM	1.8 / 1.5	0.196
VccVRM	1.05	< 1 (mA)
VccALVDS	3.3	< 1 (mA)
VccTX_LVDS	1.8	0.059

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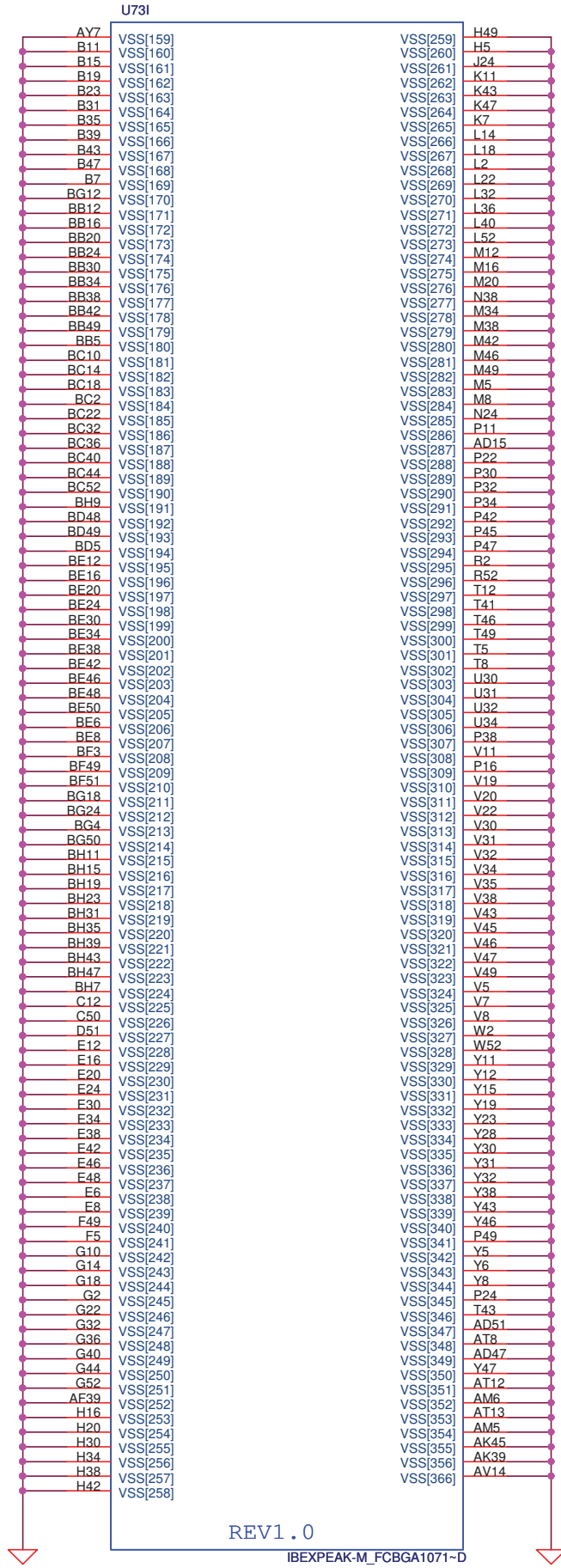
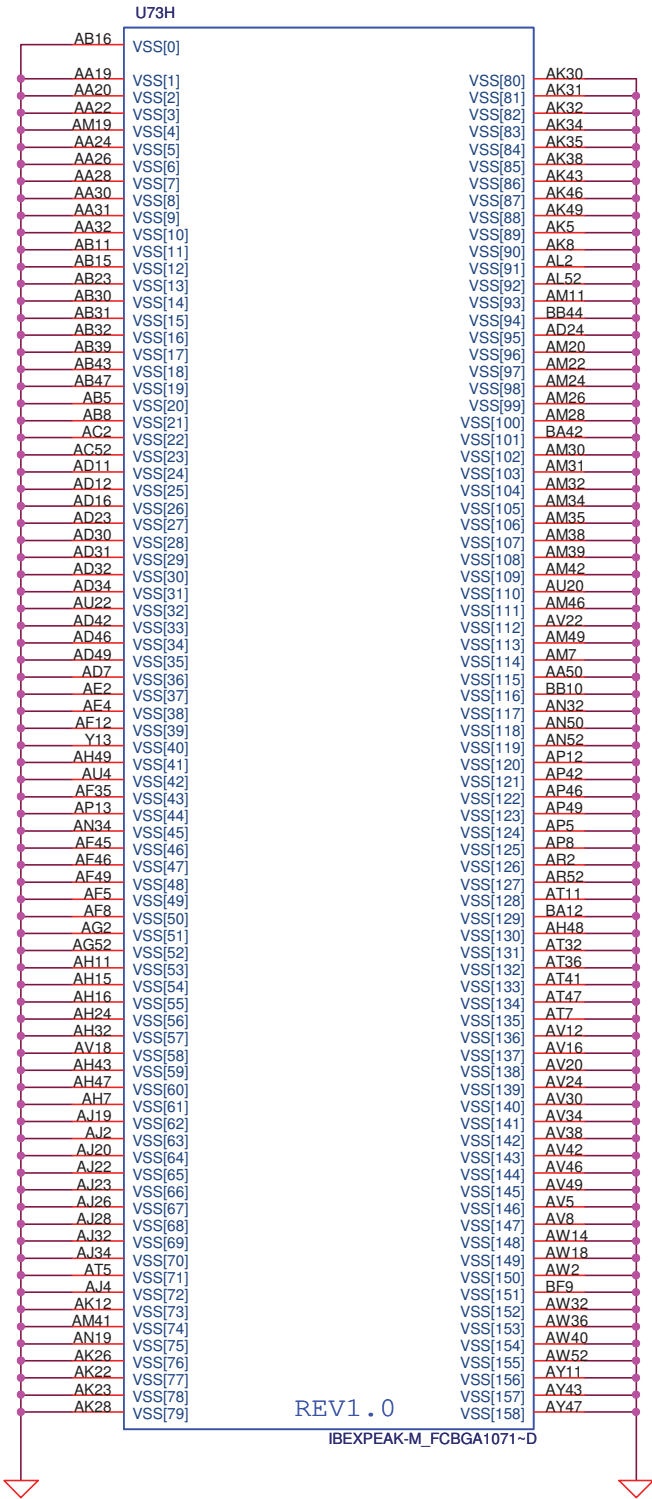
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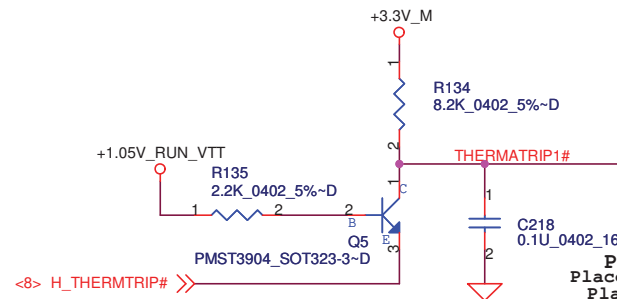
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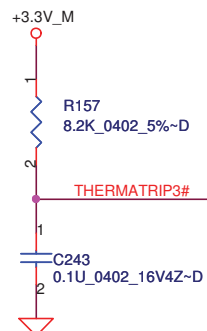
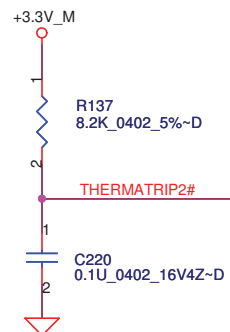




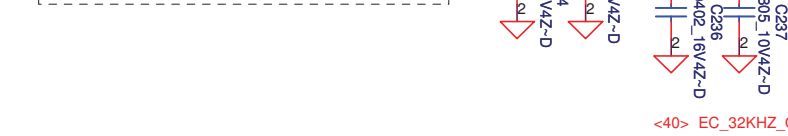
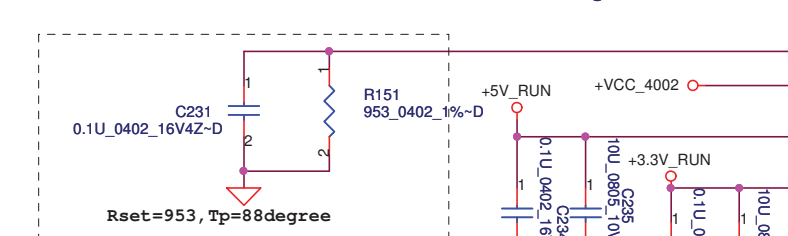
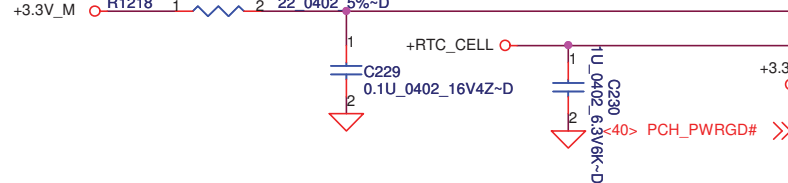
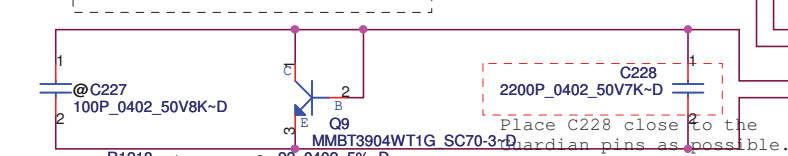
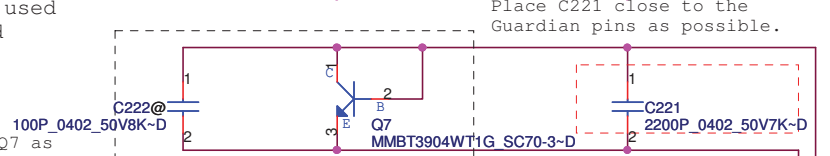
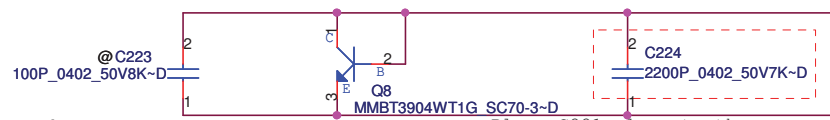
Diode circuit at DP2/DN2 is used for skin temp sensor (placed optimally between CPU, MCH and MEM).

Place C222 close to Q7 as possible.

**Q9 Place near DIMM**  
Place C227 close to Q9

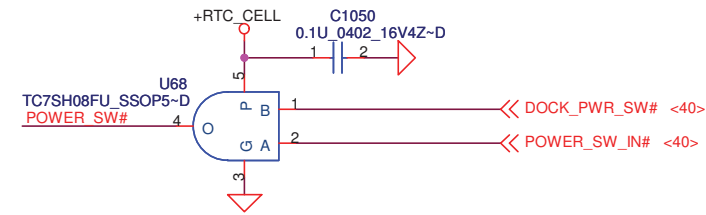
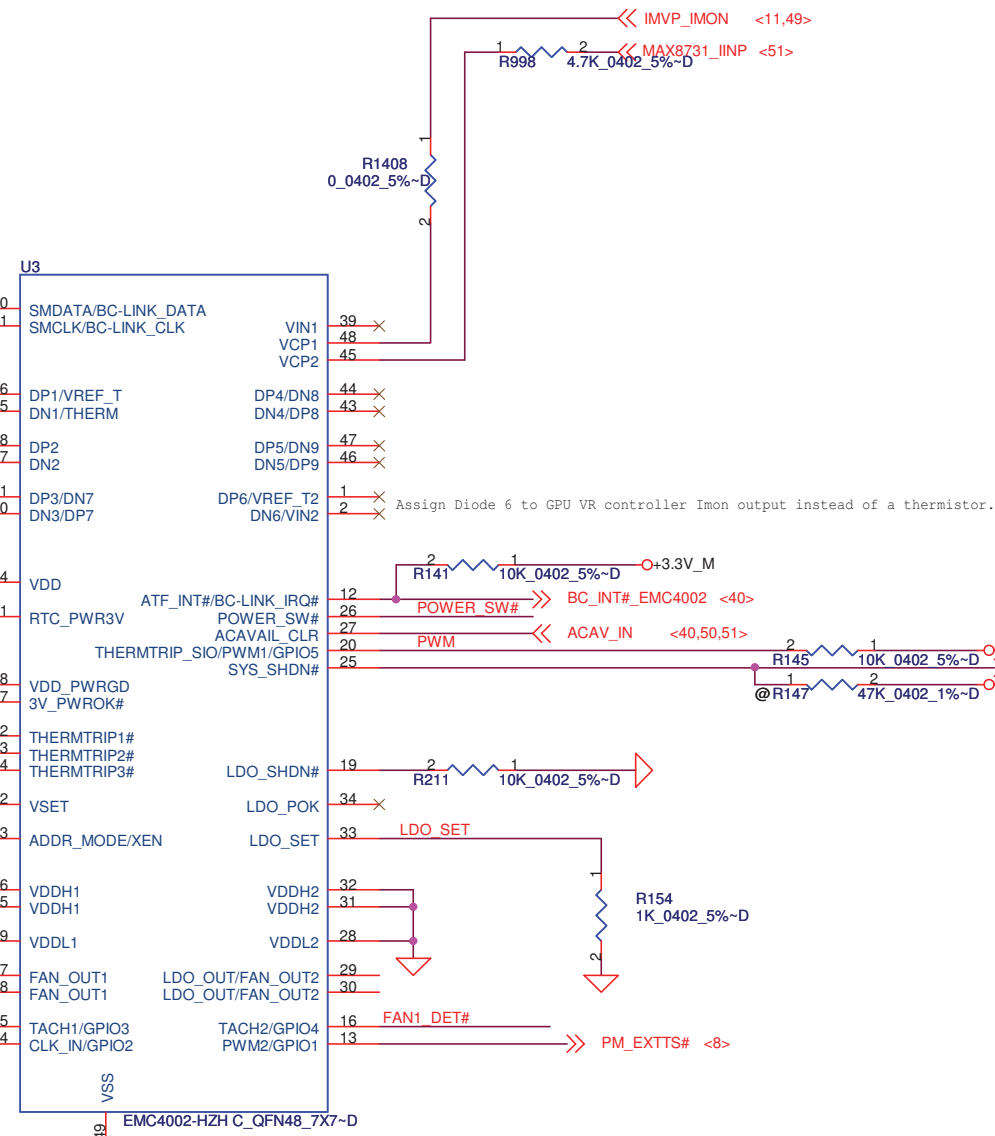
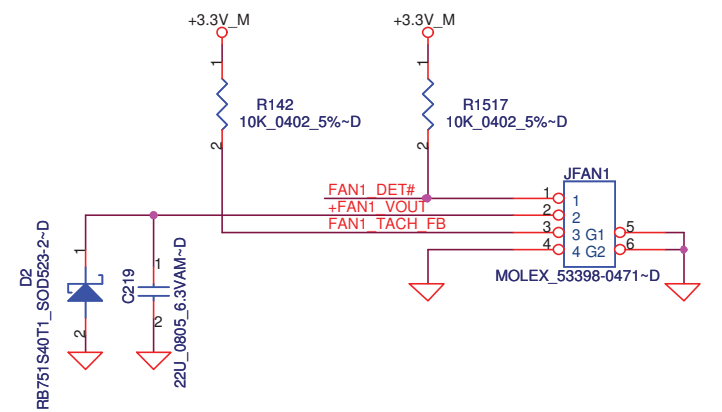


Place under CPU  
Place C223 close to the Q8 as possible  
Place C224, close to the Guardian pins as possible



Pull-up Resistor on ADDR_MODE/XEN	For Remote mode	SMBUS Address
<= 4.7K +/- 5%	2N3904	2F (r/w)
10K	2N3904	2E (r/w)
18K	Thermistor	2F (r/w)
>= 33K	Thermistor	2E (r/w)

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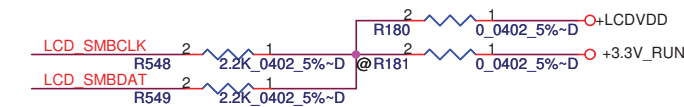
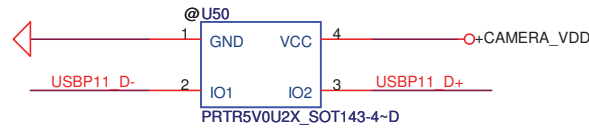
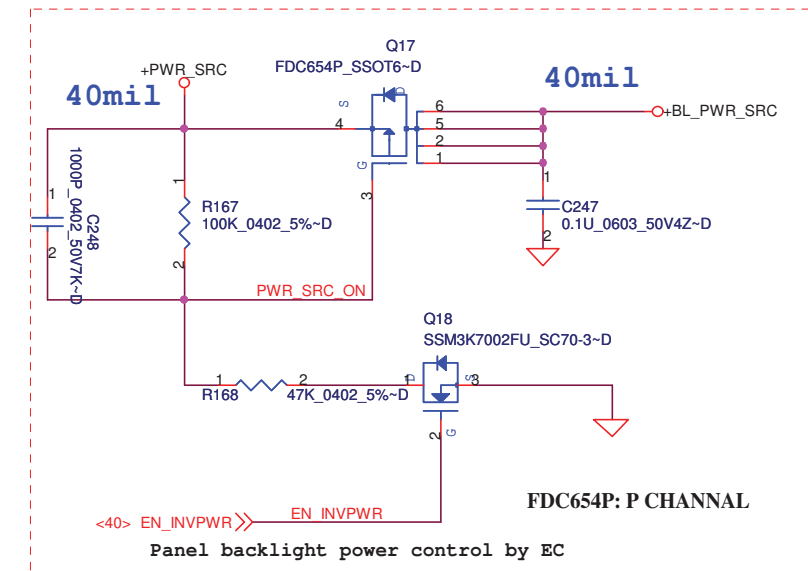
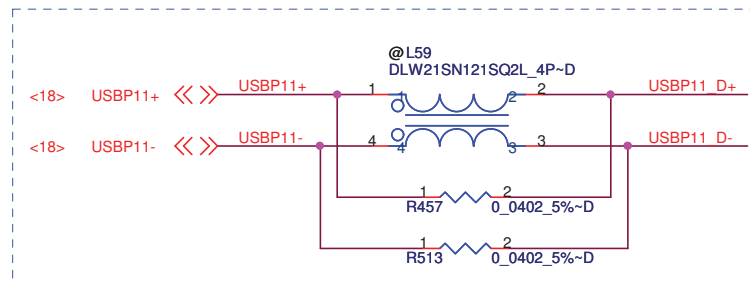
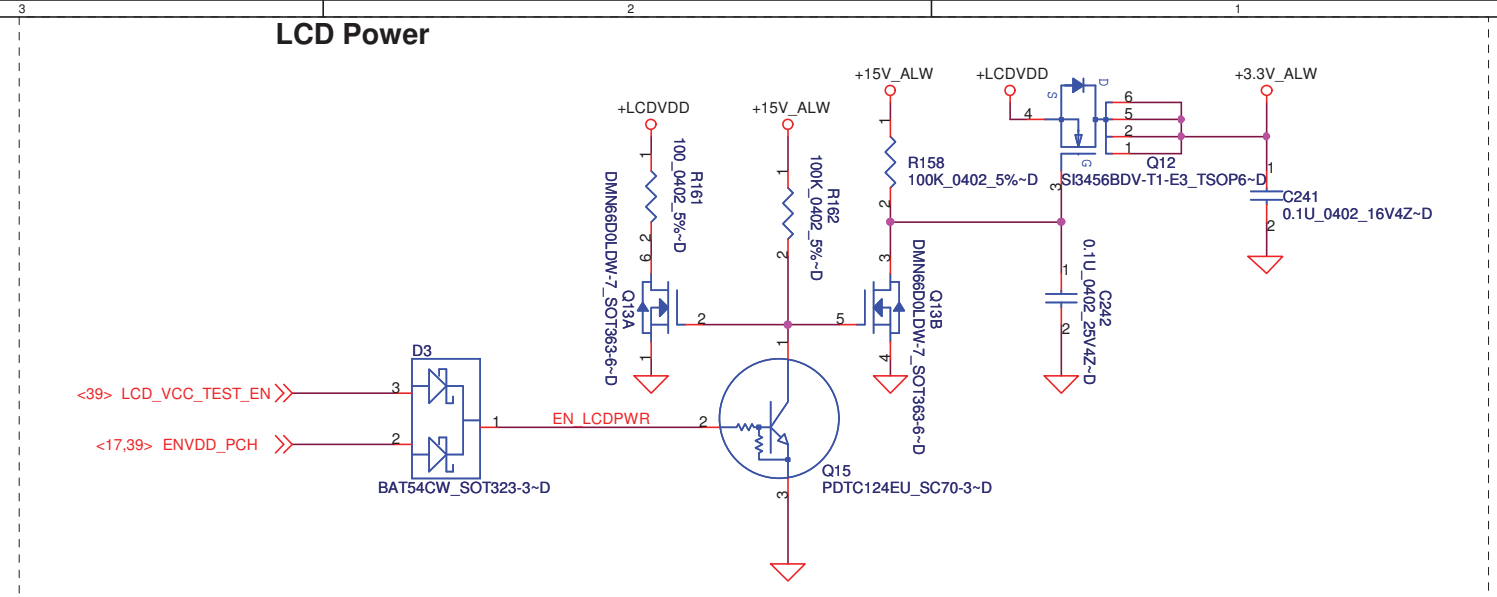
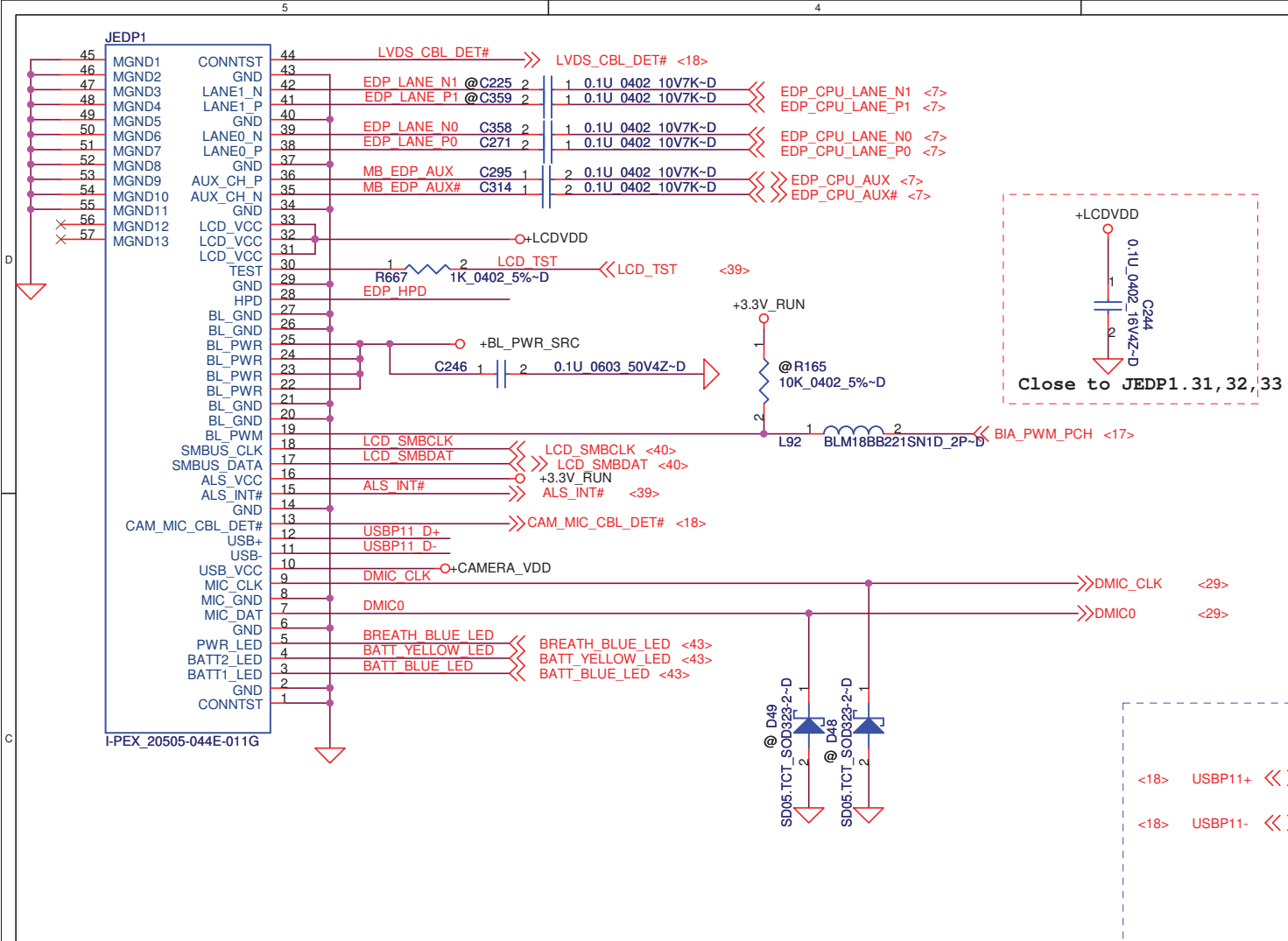
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FAN & Thermal Sensor

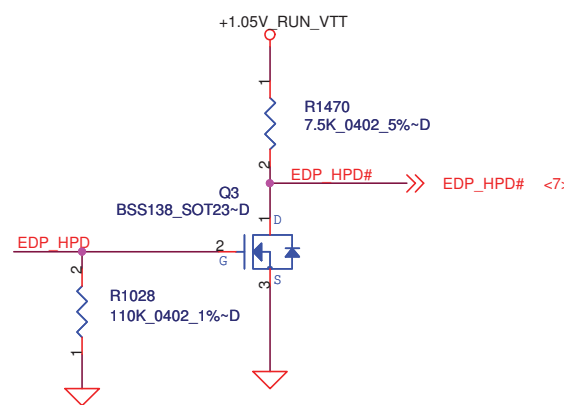
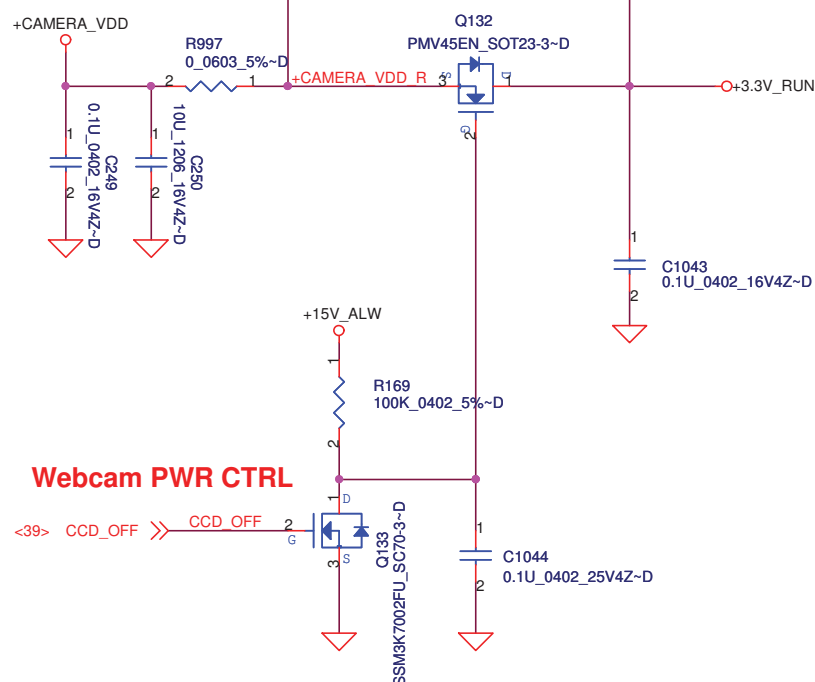
LA-5471P

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## For Webcam



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eDP & CAM Conn

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# AUX/DDC SW for DPC to E-DOCK

The schematic diagram illustrates the AUX/DDC SW for DPC to E-DOCK. It features two main integrated circuits (ICs) and several capacitors.

**IC U86 (PI3C3125LEX\_TSSOP14~D):** This 14-pin IC is connected as follows:

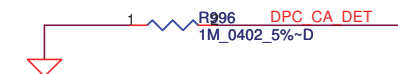
- Pins 1 and 2: DPC\_AUX C (Signal: <17> DPC\_PCH\_DOCK\_AUX << 2 1)
- Pins 3 and 4: DPC\_DOCK\_AUX (Signal: <38> DPC\_DOCK\_AUX << 2 1)
- Pins 5 and 6: DPC\_AUX# C (Signal: <17> DPC\_PCH\_DOCK\_AUX# << 2 1)
- Pins 7 and 8: DPC\_DOCK\_AUX# (Signal: <38> DPC\_DOCK\_AUX# << 2 1)
- Pin 9: GND
- Pins 10-14: PCH\_DDP\_CTRLCCLK (Signal: <17> PCH\_DDP\_CTRLCCLK << 2 1)
- Pins 15-19: PCH\_DDP\_CTRLDATA (Signal: <17> PCH\_DDP\_CTRLDATA << 2 1)
- Pins 20-24: +3.3V\_RUN

**IC U8 (NC7SZ04P5X\_NL\_SC70-5~D):** This 5-pin IC is connected as follows:

- Pin 1: +5V\_RUN
- Pin 2: DPC\_CA\_DET (Signal: <38> DPC\_CA\_DET << 2 1)
- Pin 3: DPC\_CA\_DET (Signal: <38> DPC\_CA\_DET << 2 1)
- Pin 4: DPC\_CA\_DET (Signal: <38> DPC\_CA\_DET << 2 1)
- Pin 5: GND

**Capacitors:**

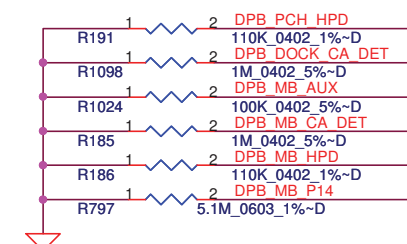
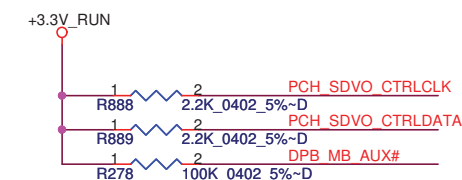
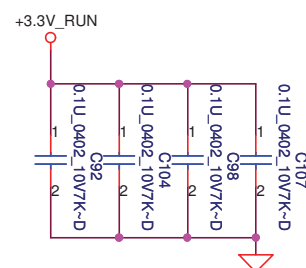
- C272: 0.1U\_0402\_10V7K~D
- C274: 0.1U\_0402\_10V7K~D
- C277: 0.1U\_0402\_16V4Z~D
- C337: 0.1U\_0402\_16V4Z~D



Title			
<b>DPC DPD SW for DOCK</b>			
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The schematic shows two identical components, C1893 and C1894, connected in parallel. Each component is represented by a capacitor symbol with pins 1 and 2. Pin 1 is connected to the positive supply rail, and pin 2 is connected to ground. The components are labeled C1893 and C1894 respectively.

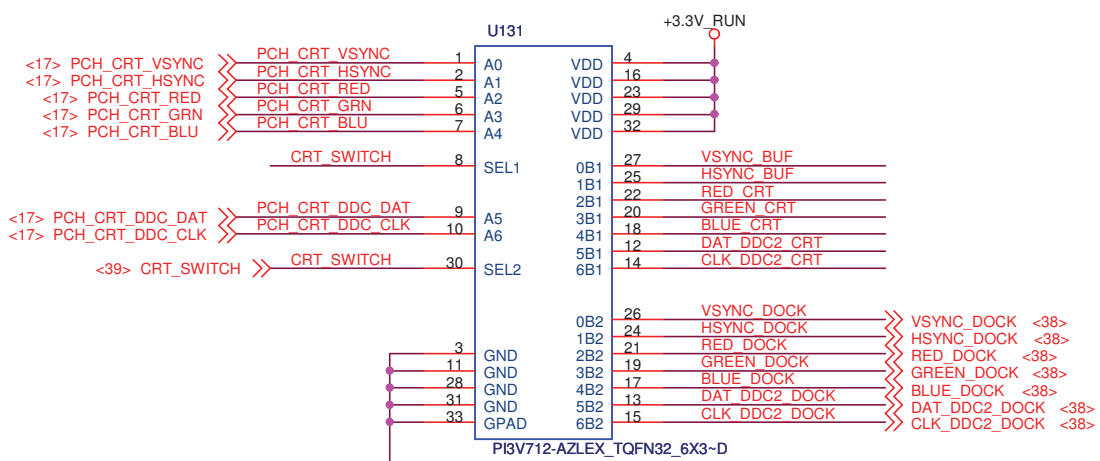


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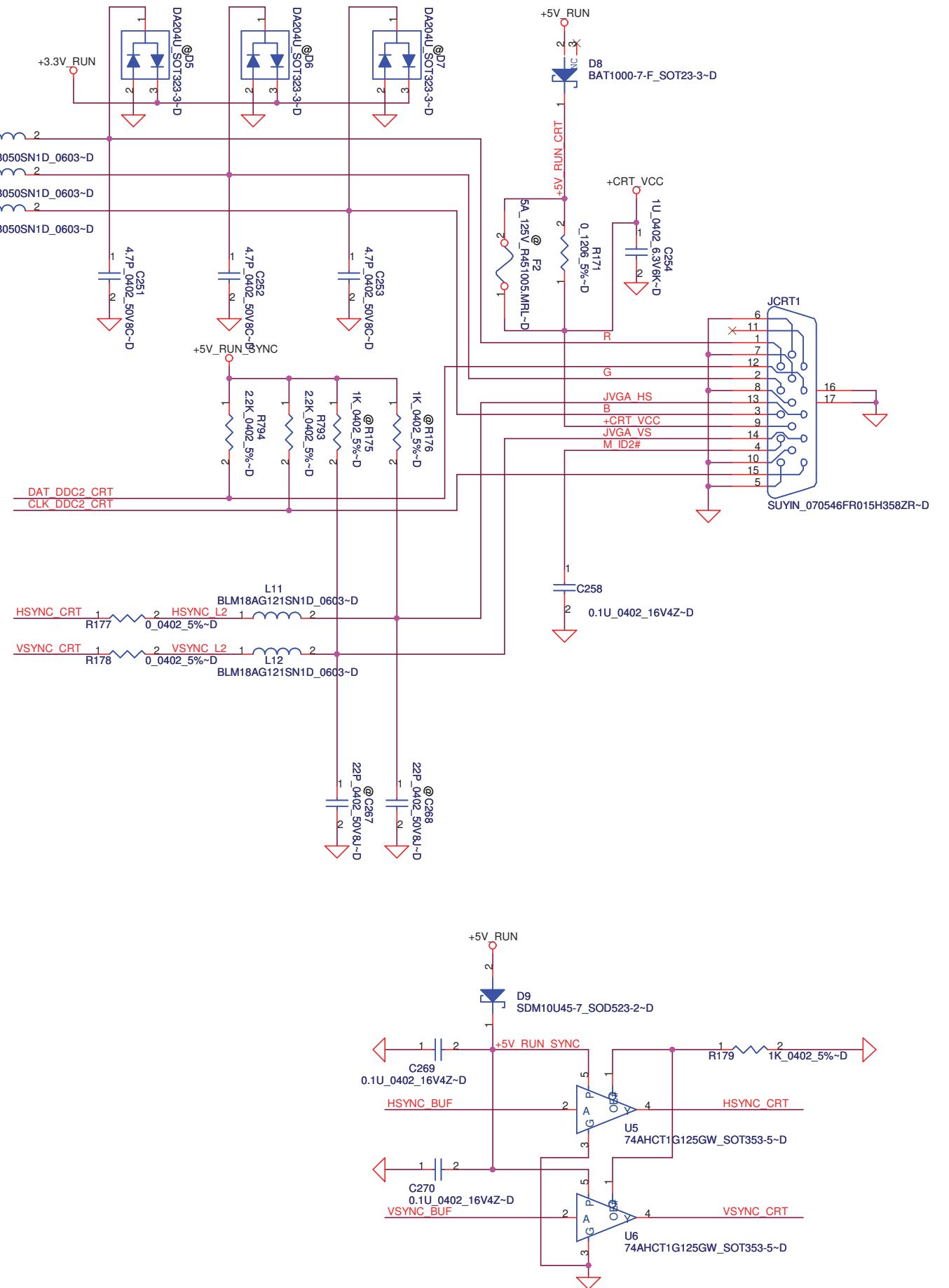
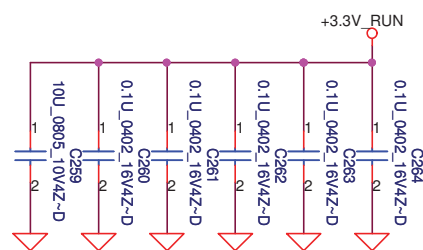
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Title			
<b>Display port</b>			
Size	Document Number		Rev
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## VGA SW for MB/DOCK



SEL	CRT
0	MB (A=B1)
1	APR/SPR (A=B2)



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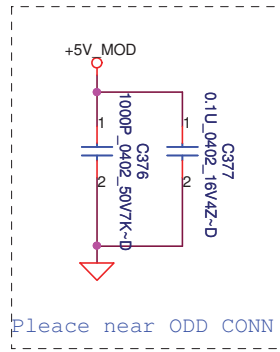
CRT/Video switch

LA-5471P

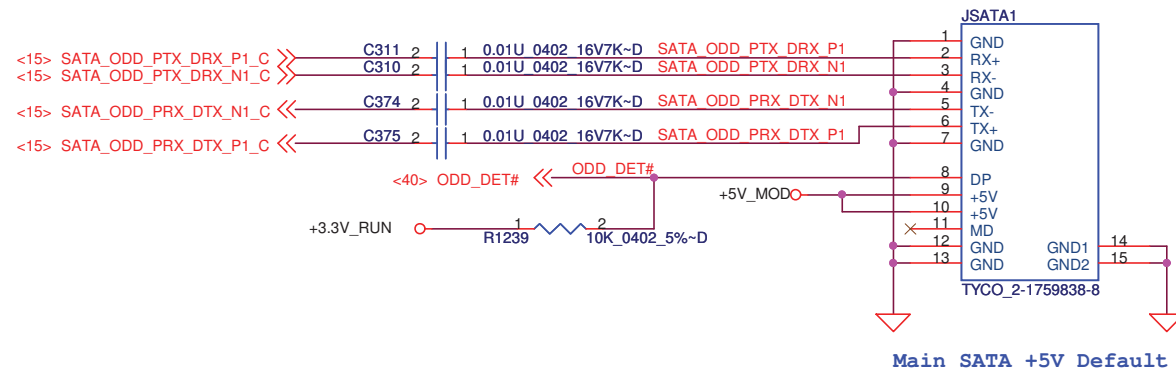
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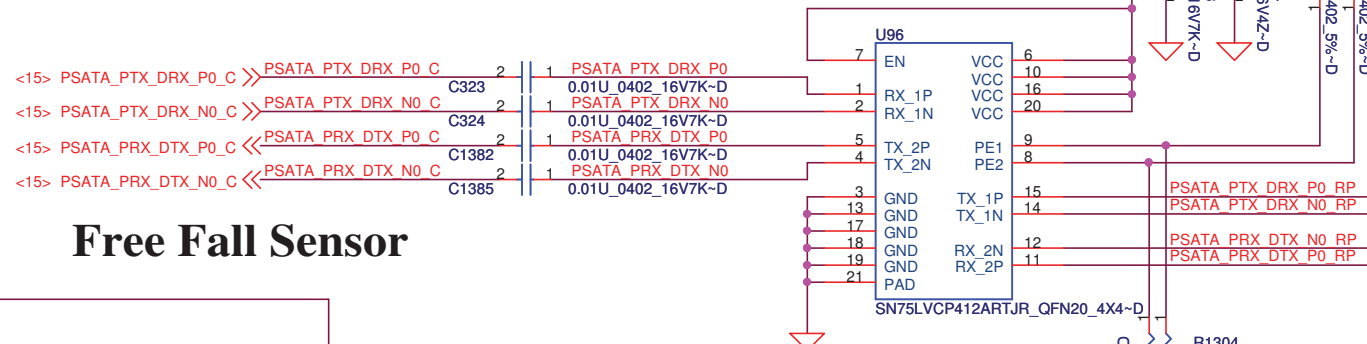
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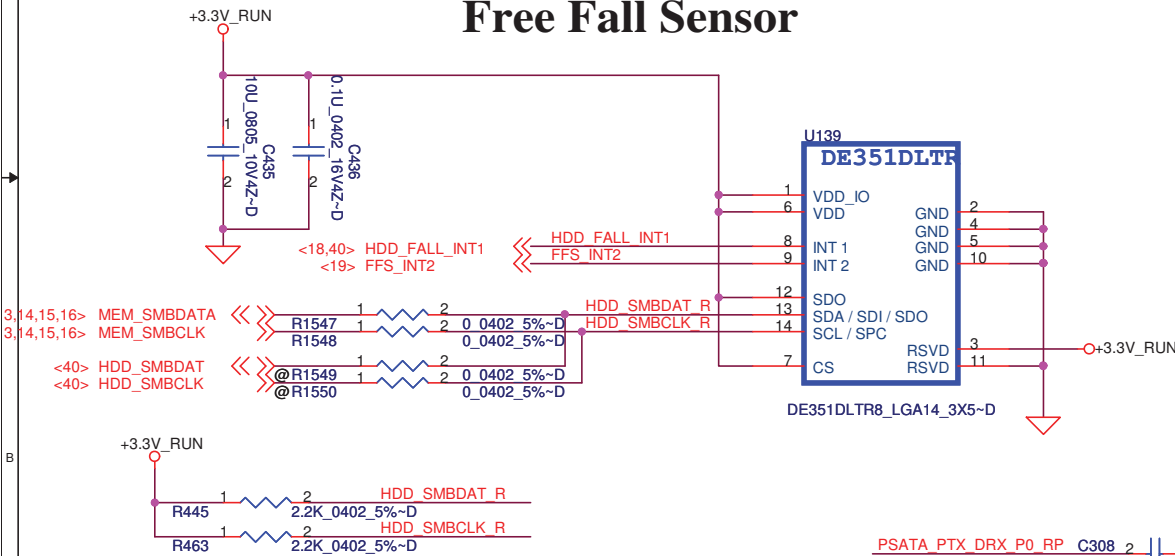
## For ODD



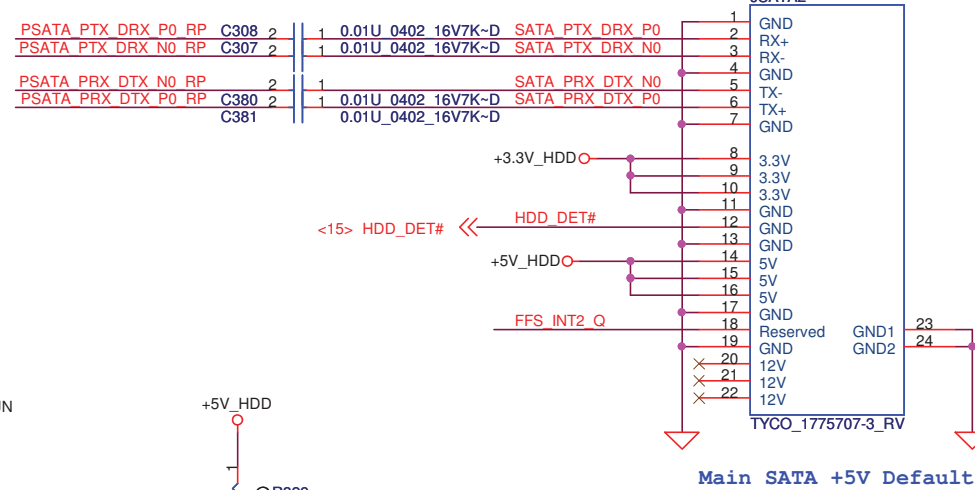
## HDD Repeater



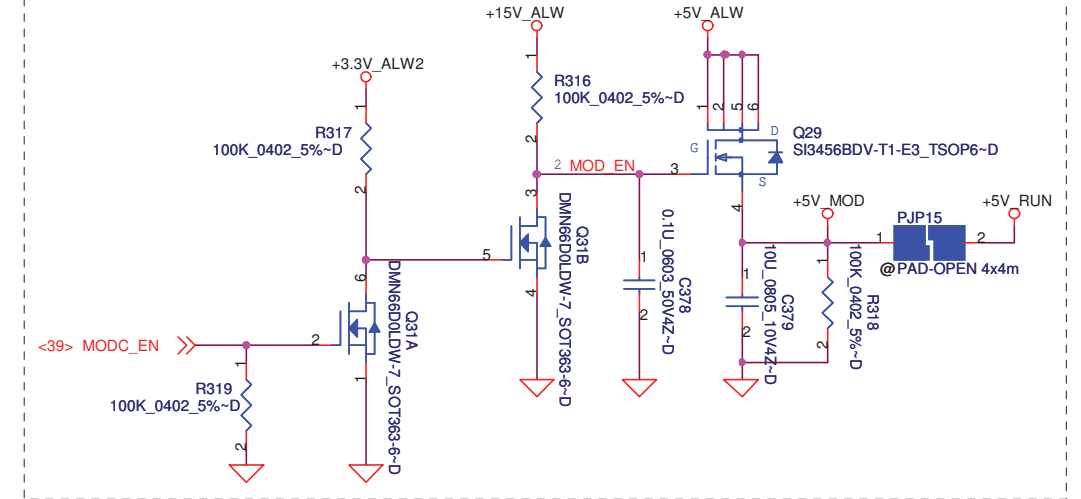
## Free Fall Sensor



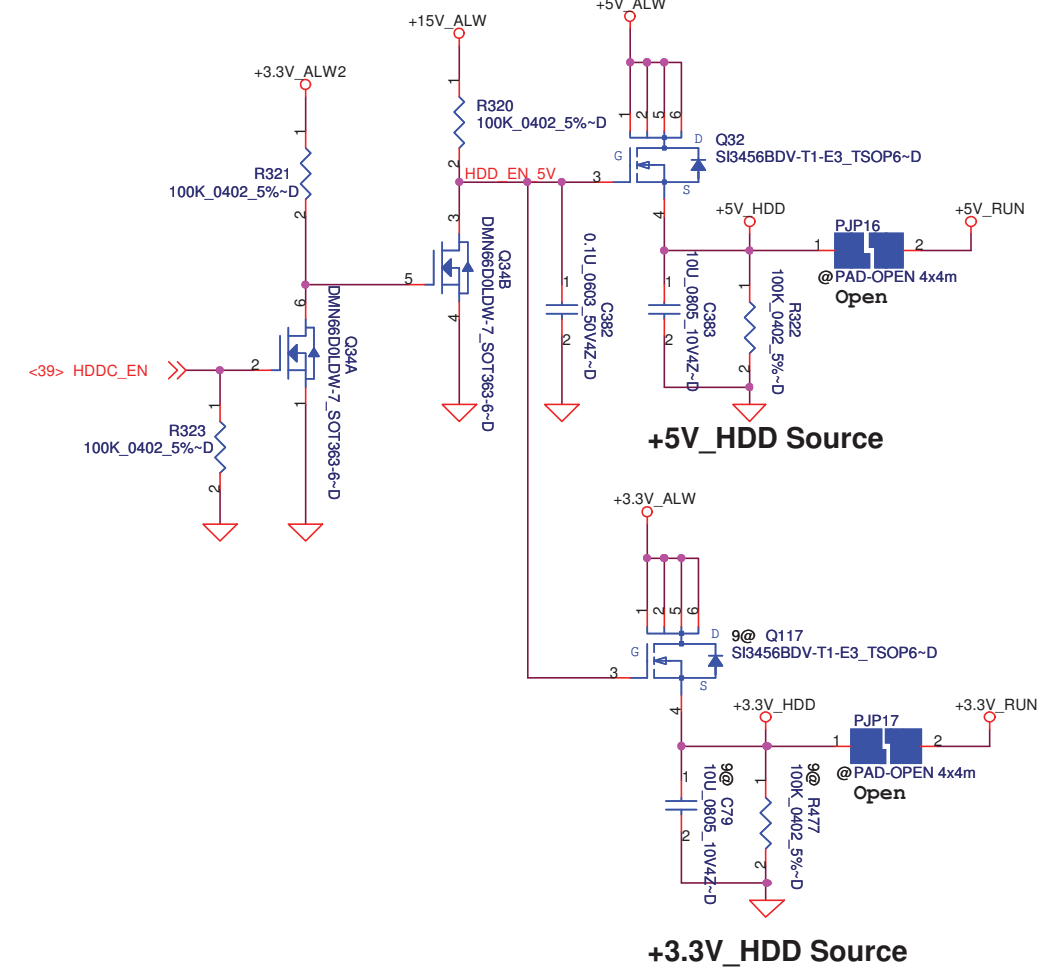
## For HDD



## +5VMOD Source



## HDD PWR



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ODD/HDD CONNECTOR

LA-5471P

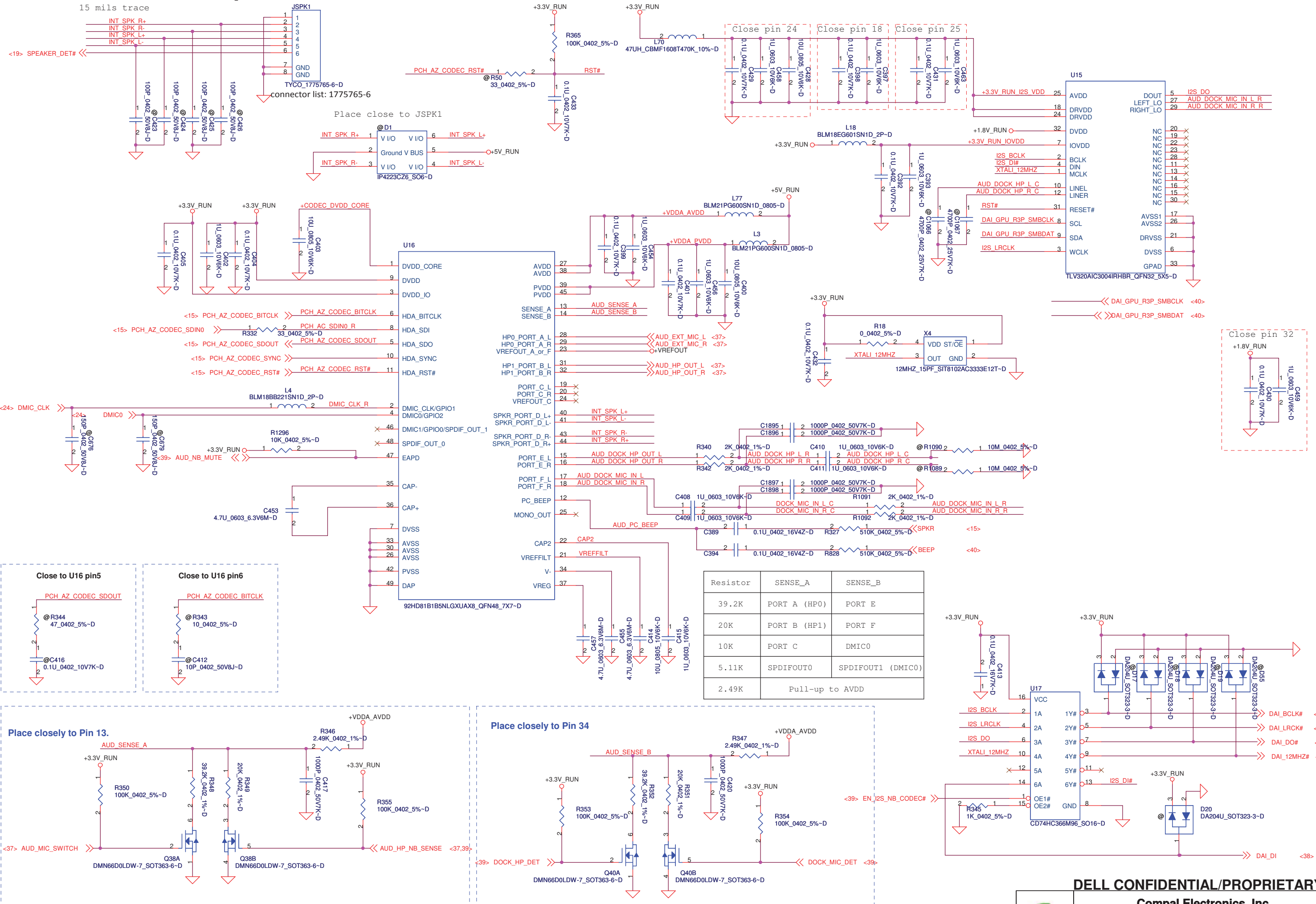
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# Speaker Connector



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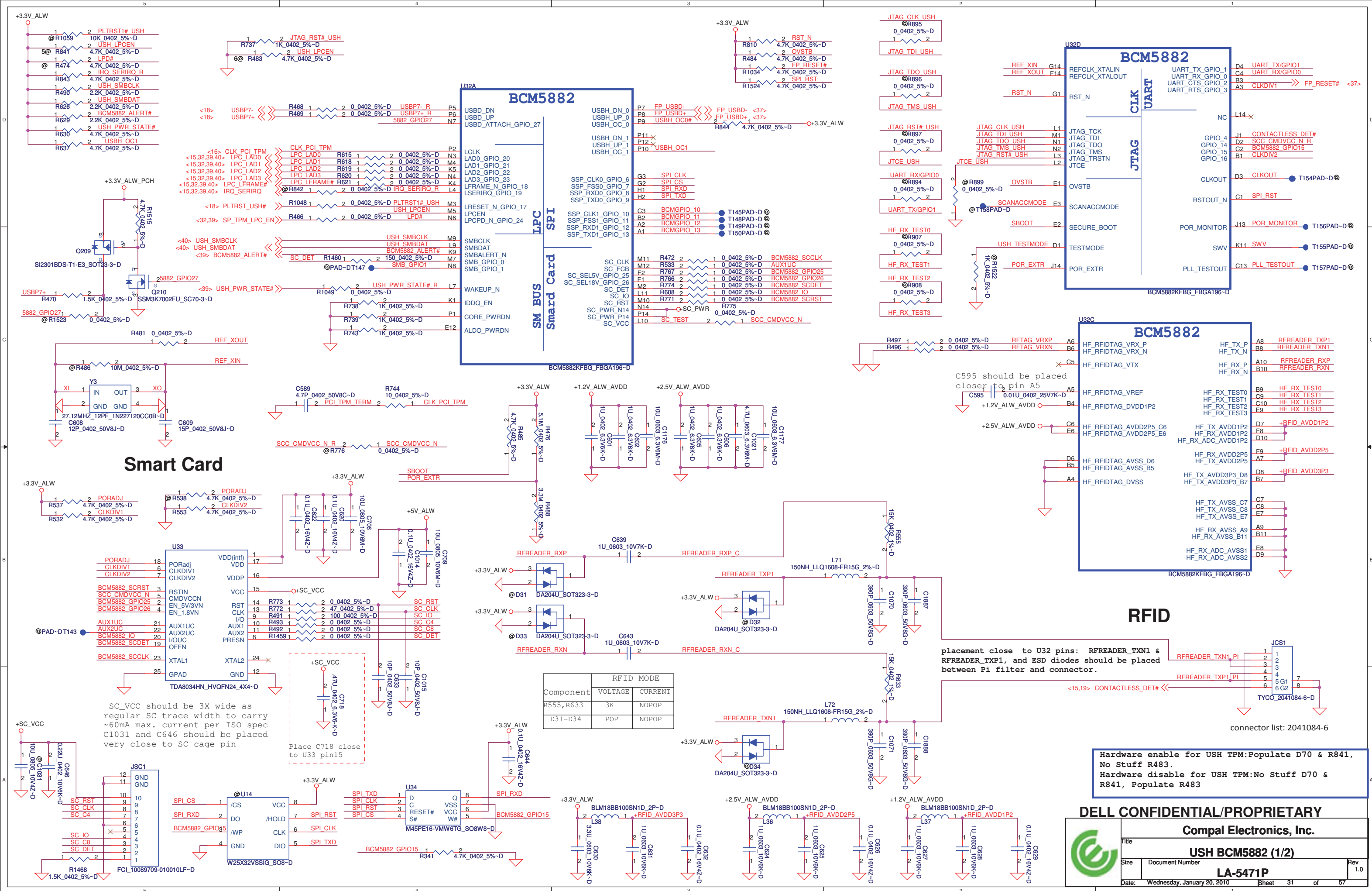
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Azalia (HD) Codec

LA-5471P

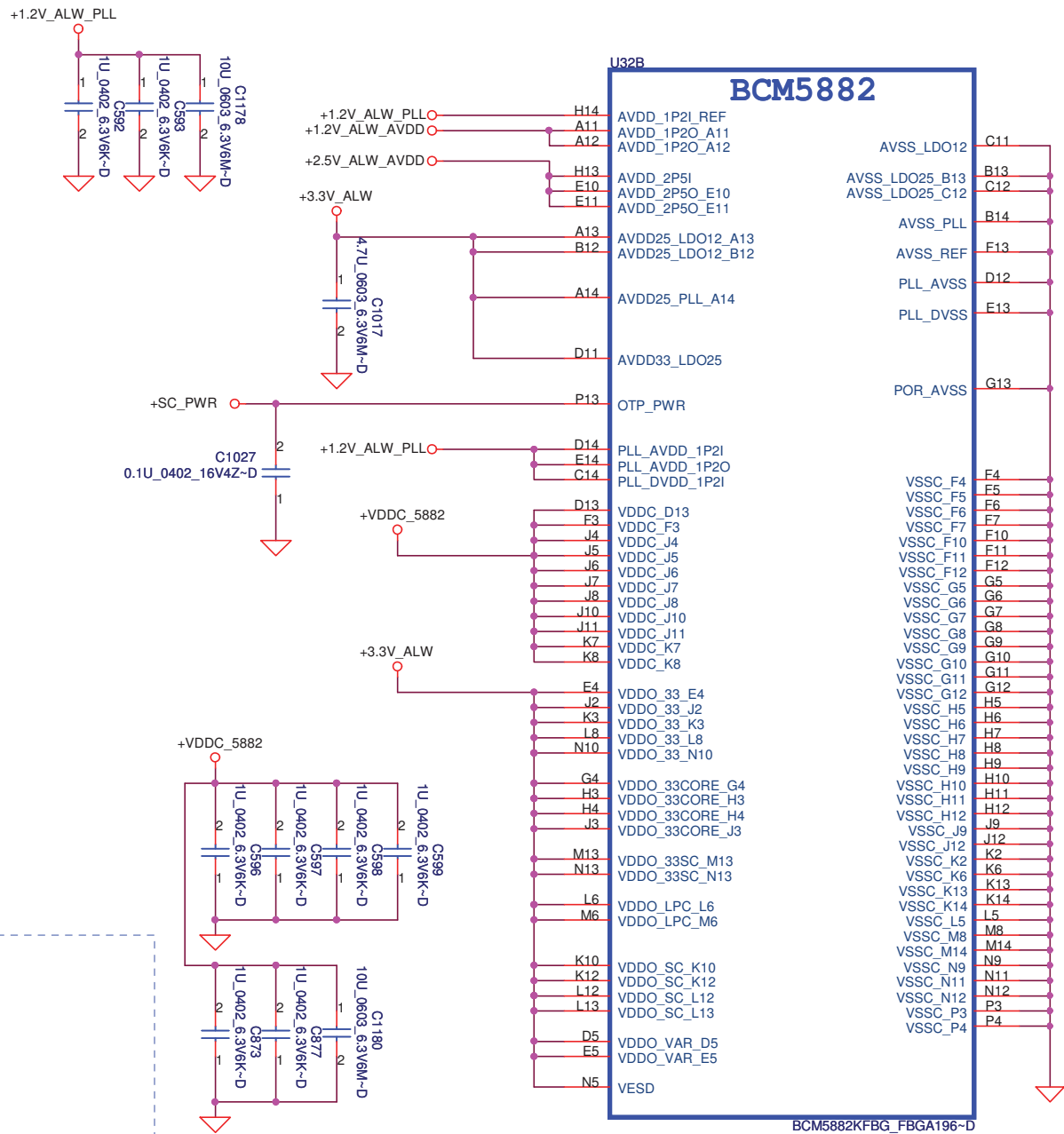
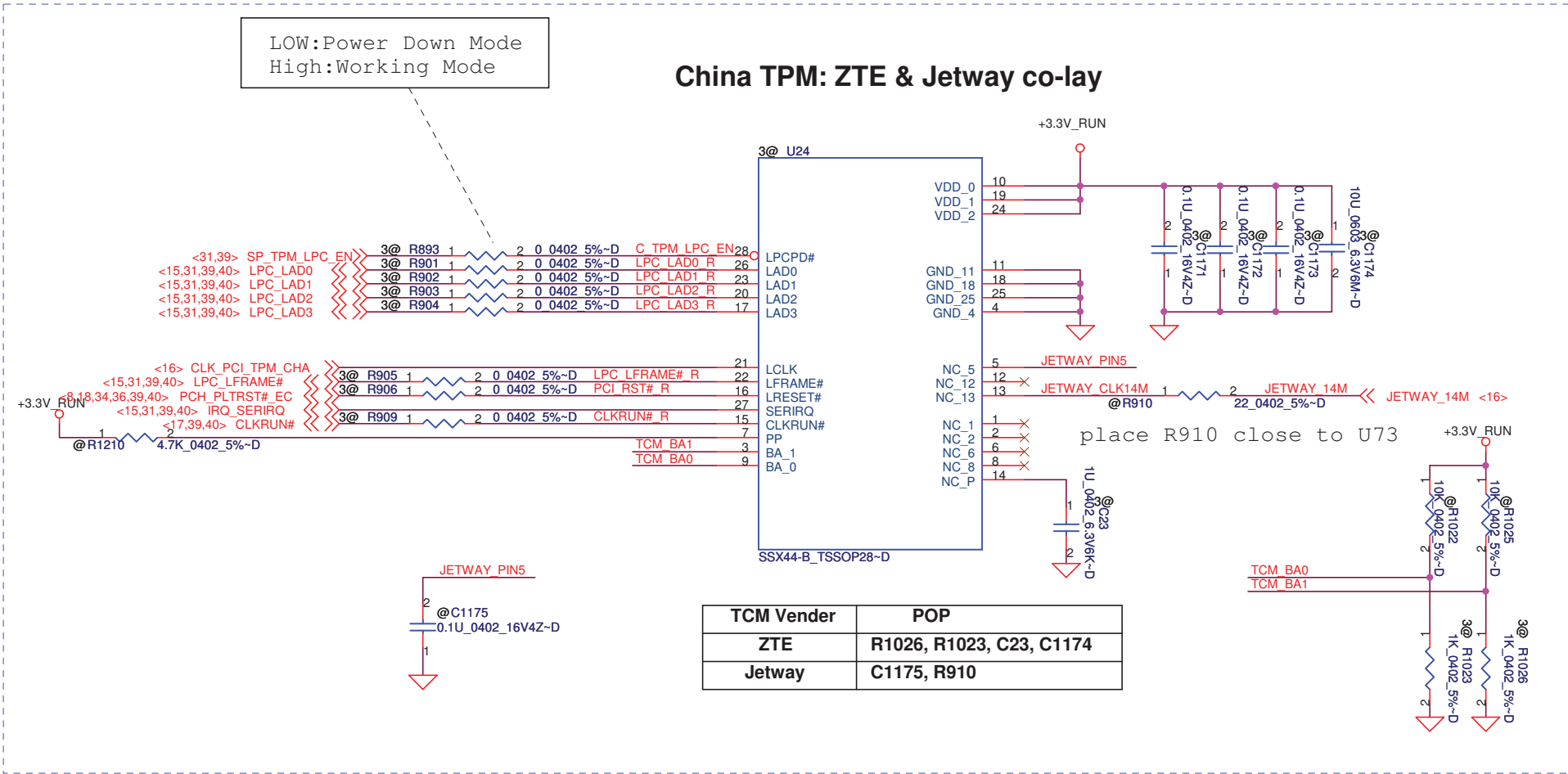
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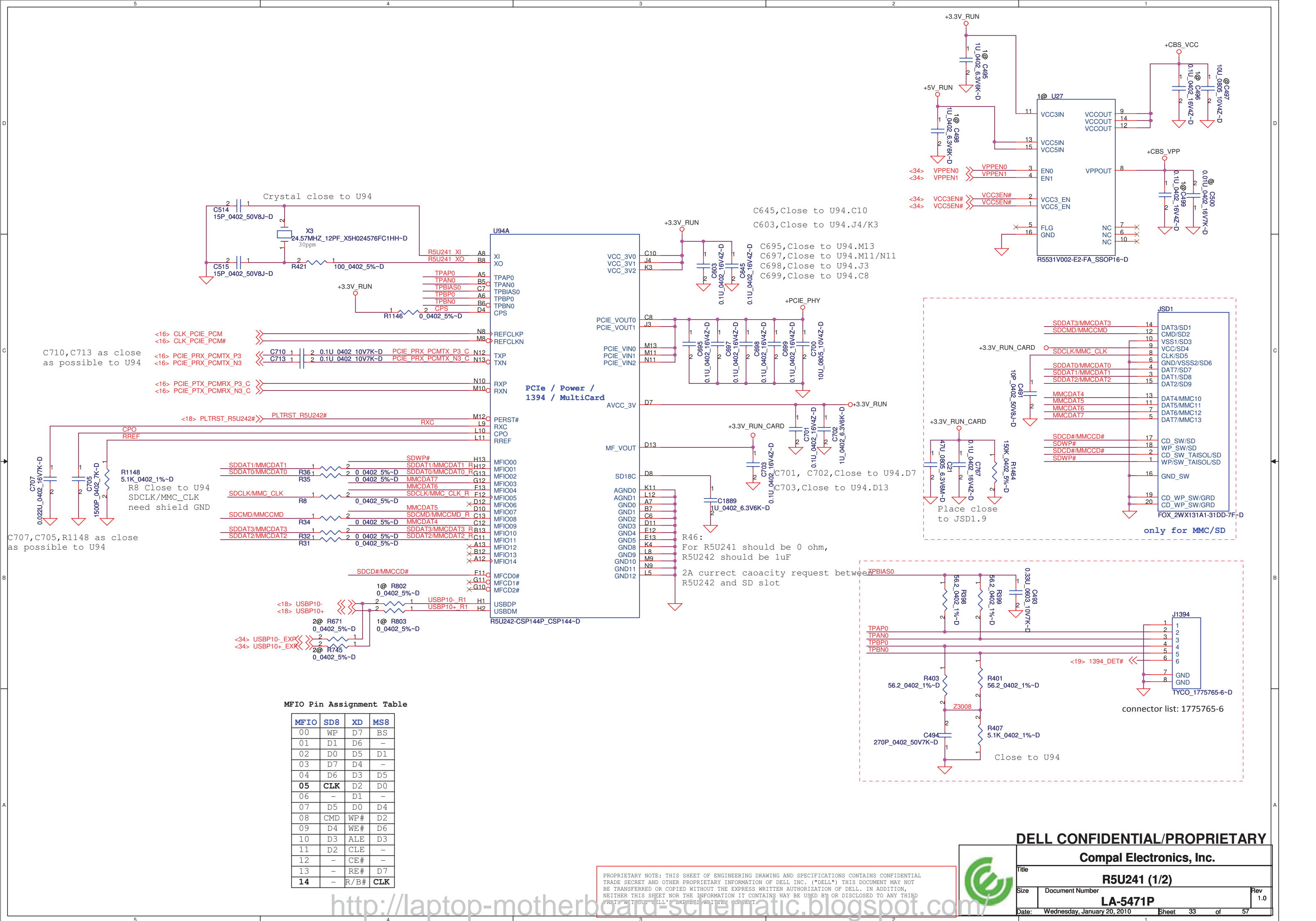


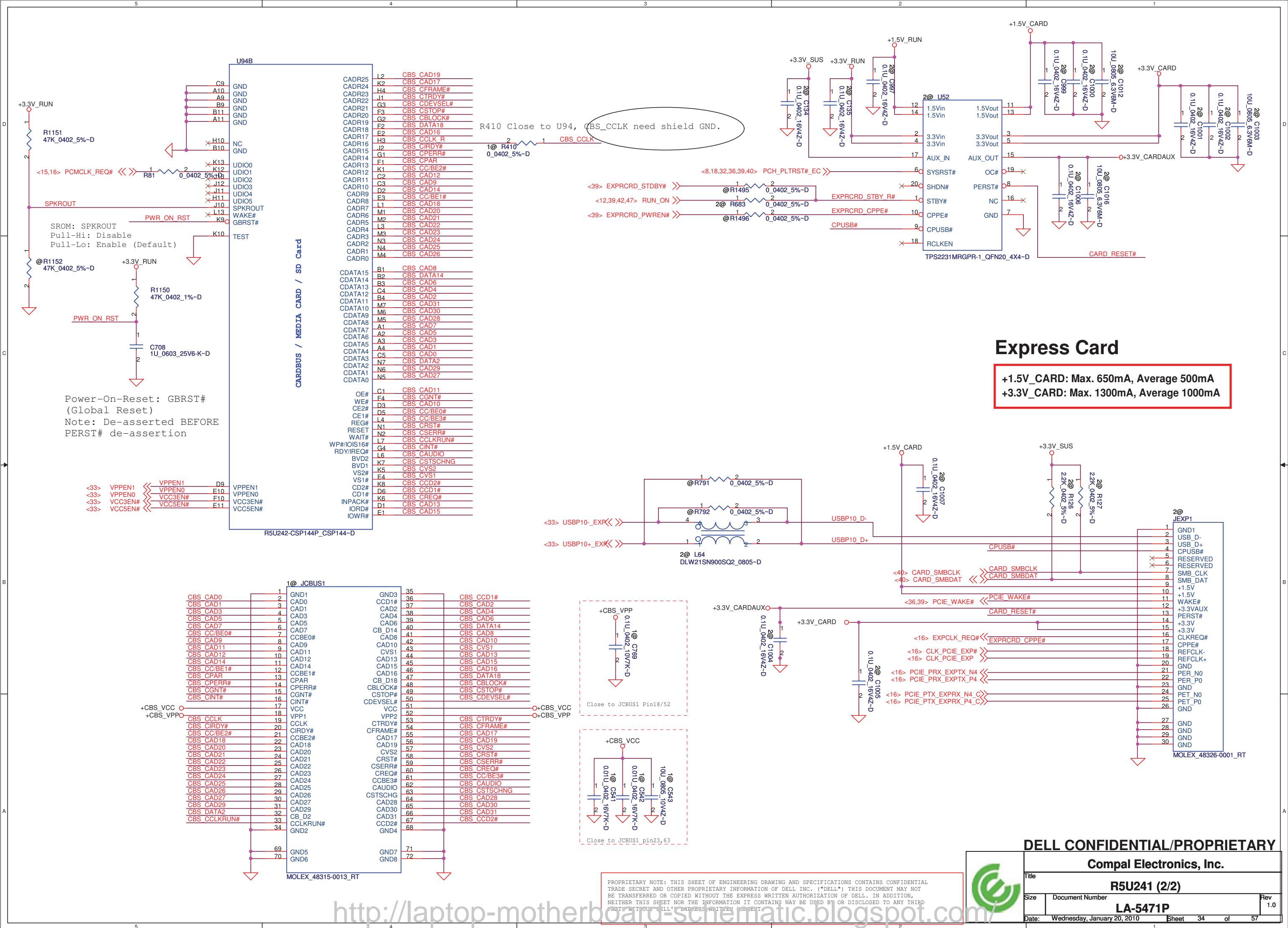


USH BCM5882 and China TPM Z8H172T Option				
PART/PIN	Ref Des	TCM Enable	TPM Enable	ALL TPM/TCM Disable
TCM circuit	All 3@	POP	@	@
SIO 5028 ->SP_TPM_LPC_EN	PU R841	@	POP	@
	PD R483	POP	@	@
	PU R788	@	@	@
PCH GPIO39 ->TPM_ID1	PU R787	@	@	POP
	PD R339	POP	POP	@
PCH GPIO38 ->TPM_ID0	PU R273	POP	POP	@
	PD R922	@	@	POP

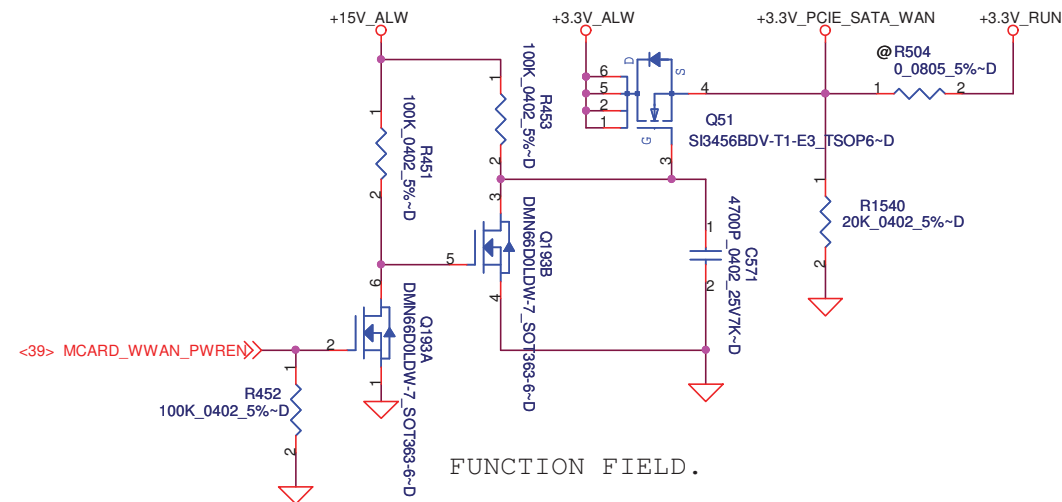




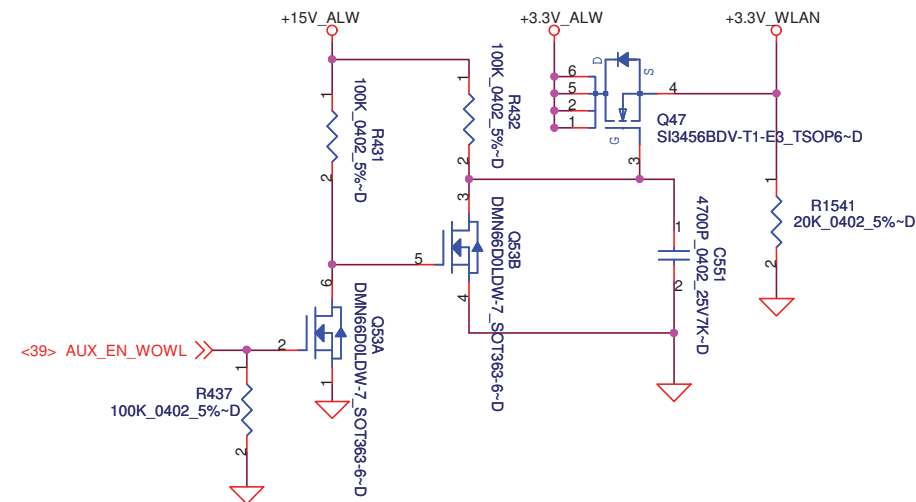




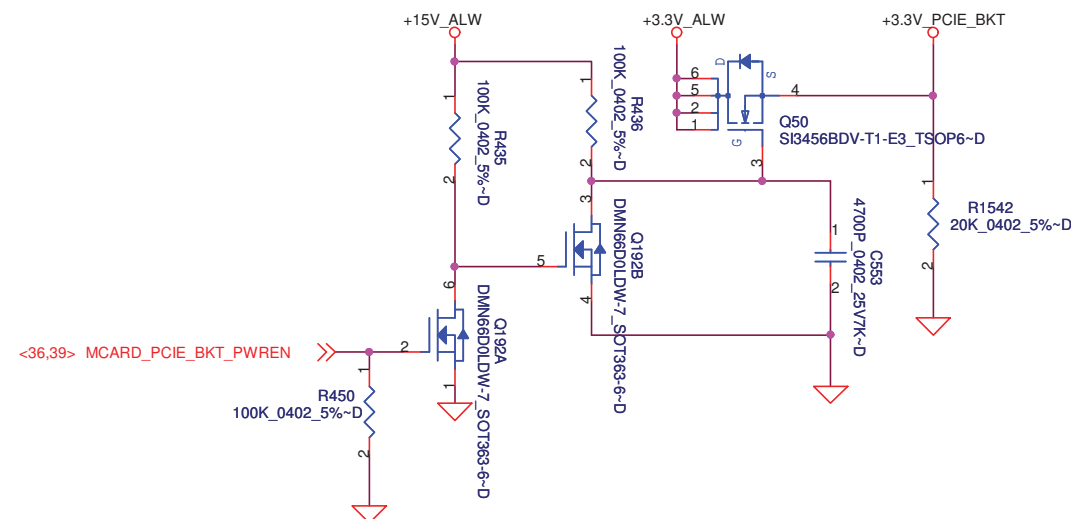
## Mini WWAN



## Mini WLAN



## PCIE/BKT Card



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Title			PCIE PWR
Size	Document Number	LA-5471P	
Date:	Wednesday, January 20, 2010	Sheet	35 of 57
		Rev	1.0

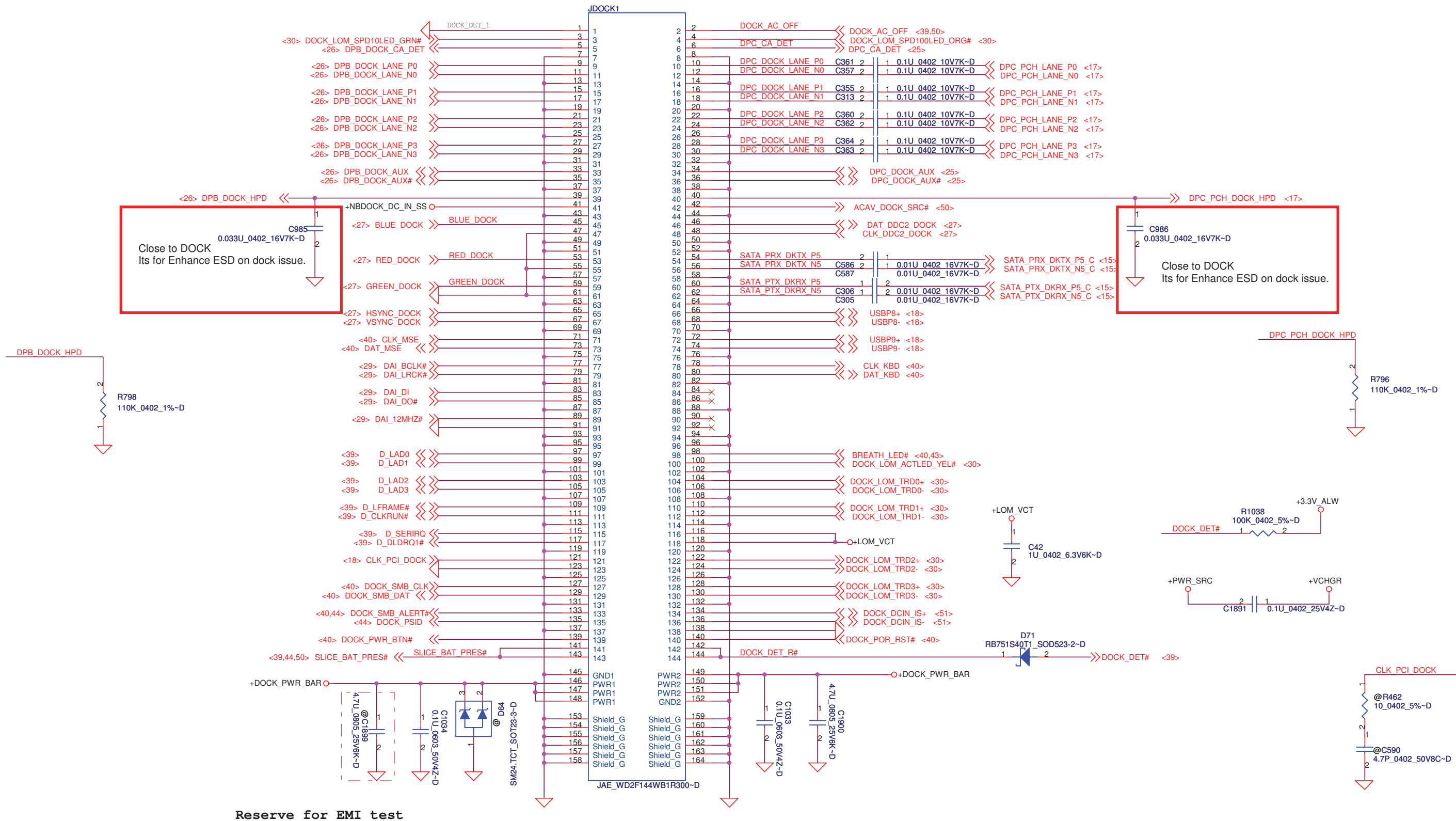
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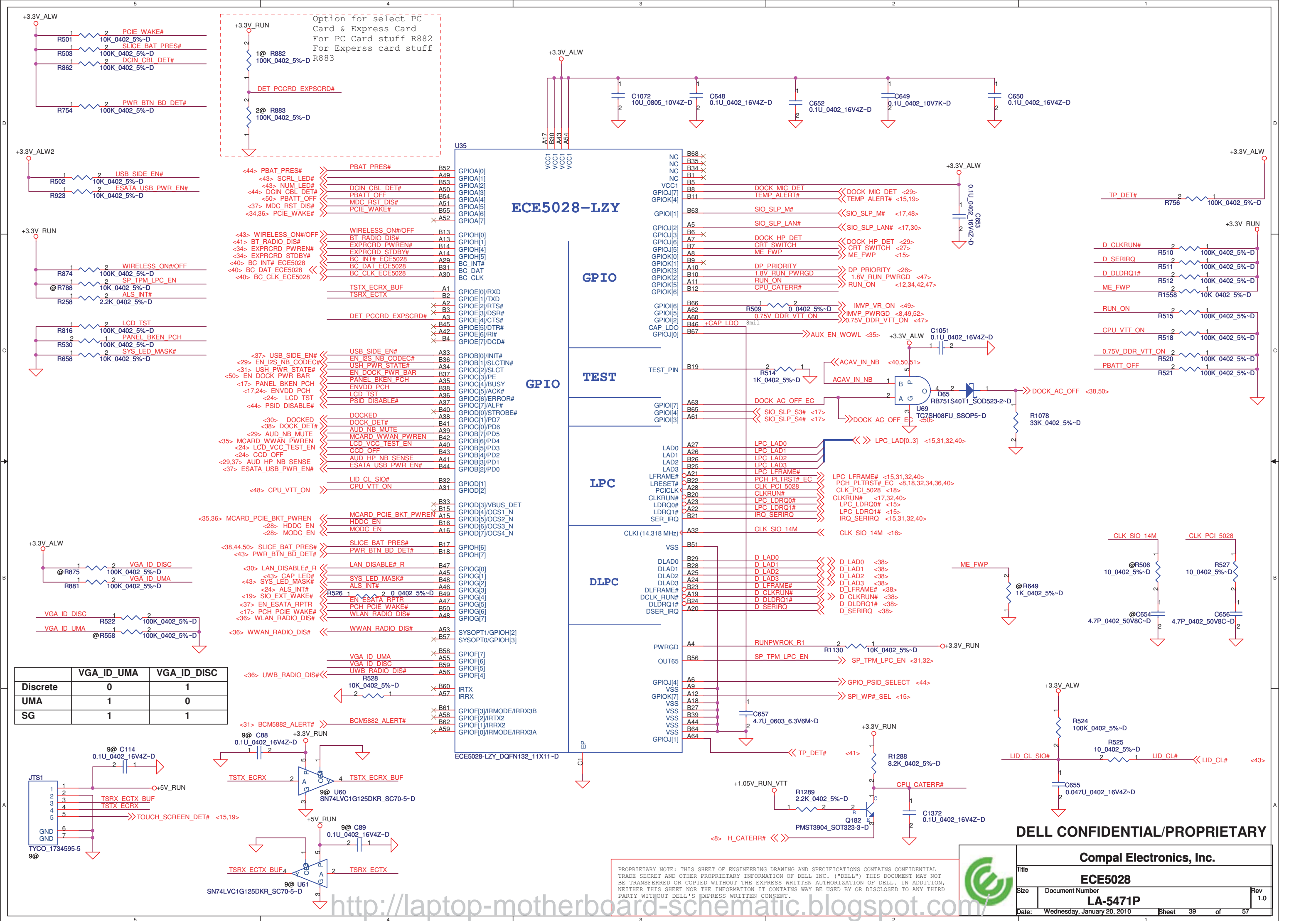




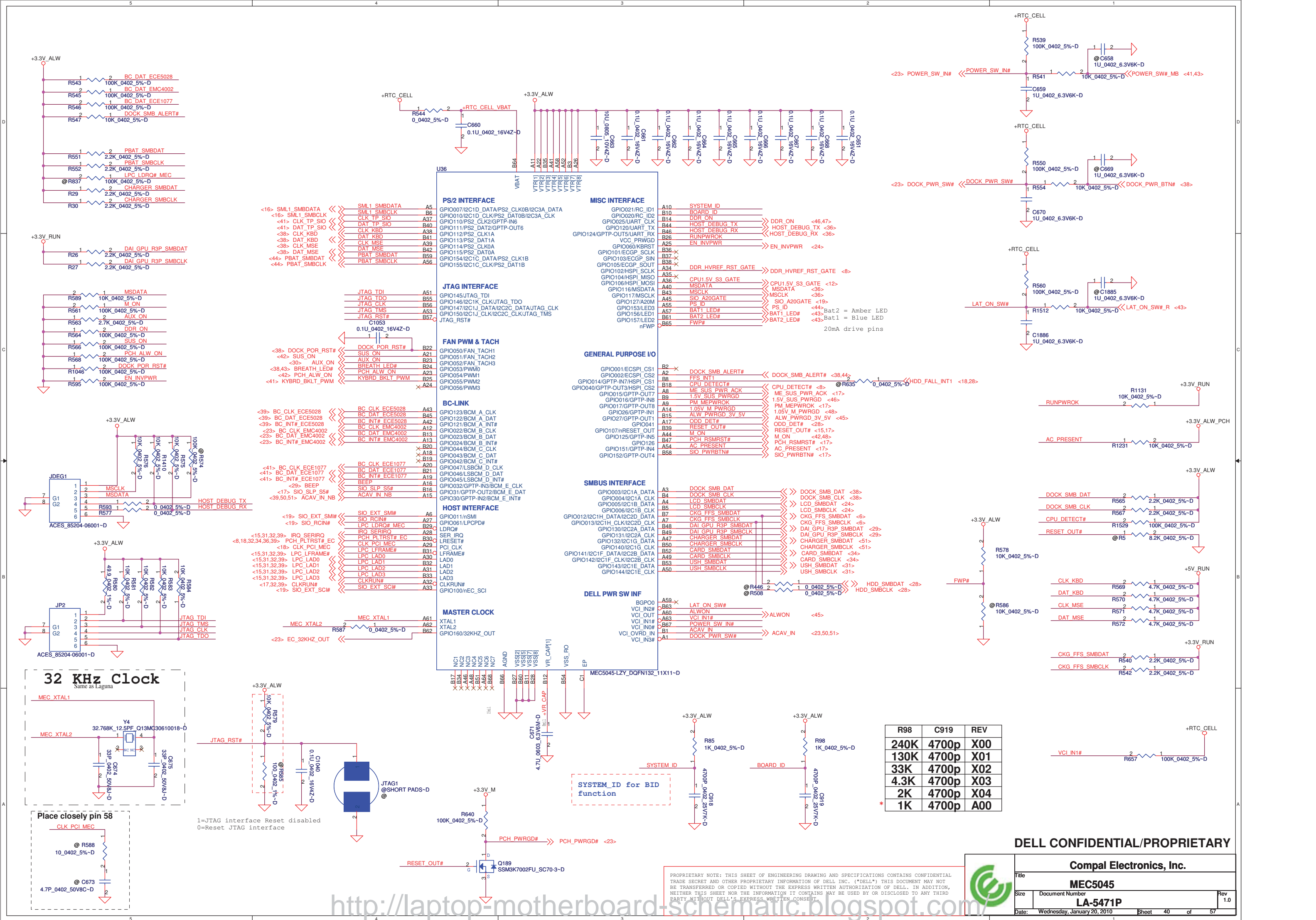
Reserve for EMI test

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Compal Electronics, Inc.			
Title		DOCKING CONN	
Size	Document Number	LA-5471P	
Date:	Wednesday, January 20, 2010	Sheet	38 of 57

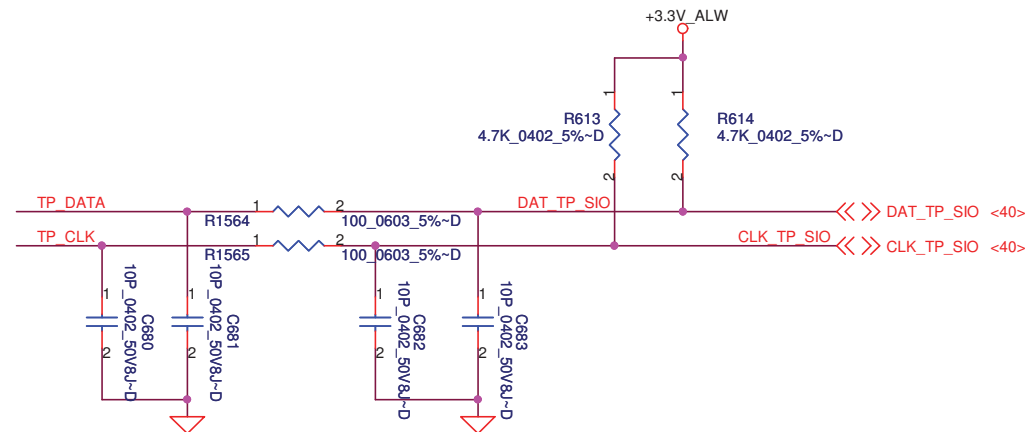




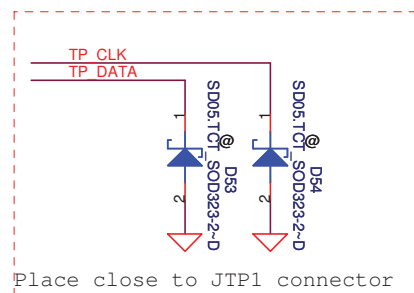
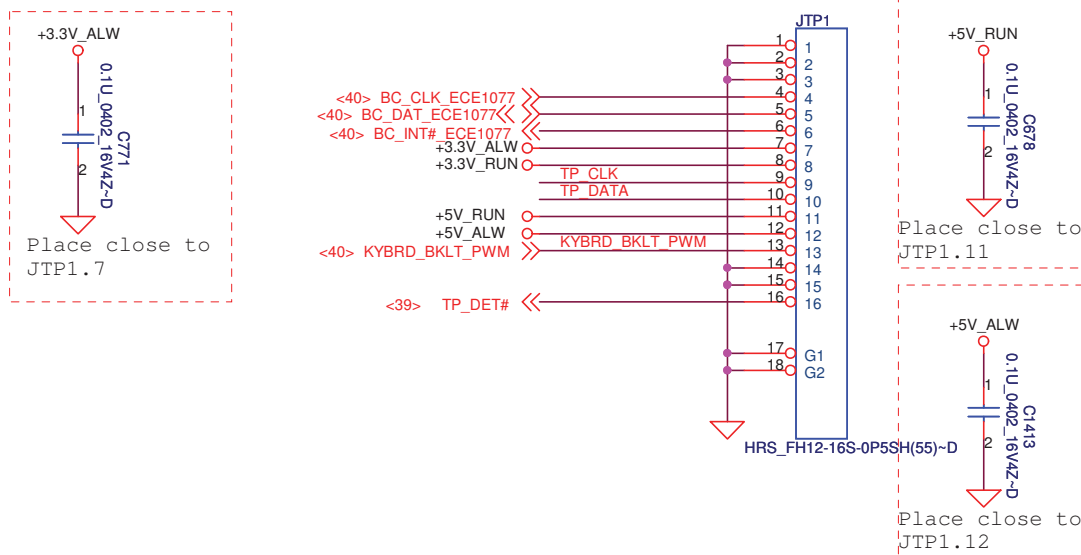




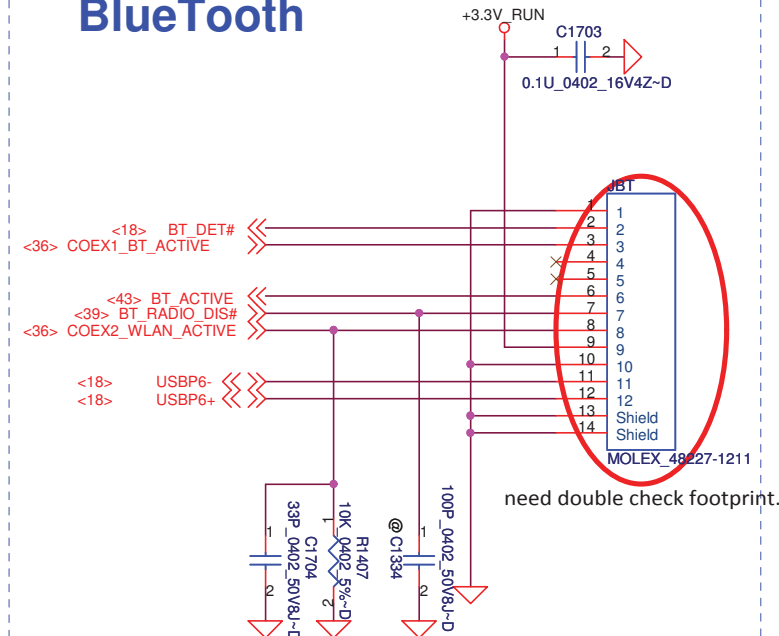
## Touch Pad



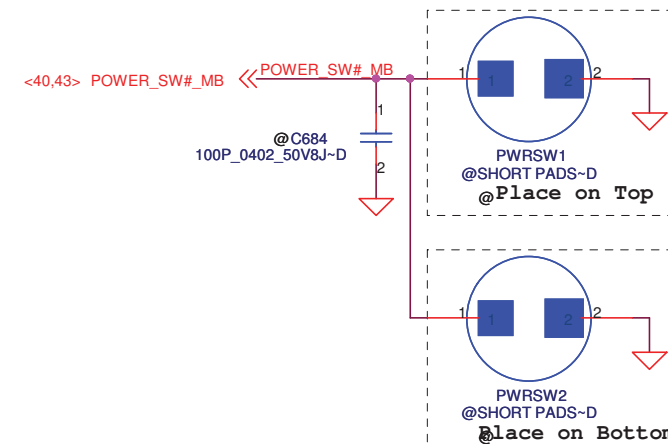
## Touch Pad Conn. Pitch=0.5



## BlueTooth



## Power Switch for debug



### @ FAN

Part Number	Description
DC28A000800	FAN SET DAQ20 DC5V AB7405HB-HB3 ADDA

### @ Speak

Part Number	Description
PK230003Q0L	SPK PACK ZJX 2.0W 4 OHM FG

### @SM CARD BODY

Part Number	Description
SP070007V0L	S SOCKET TYCO 1770551-1 10P H5.9 SMART

### @PCMCIA BODY

Part Number	Description
DC000001Q0L	PCMCIA TYCO 1759096-1

### @ MDC wire set cable

Part Number	Description
DC02000CS0L	H-CONN SET ZGX MB-MDC

### @ T/P wire set cable

Part Number	Description
DC02000840L	H-CONN SET ZJX MB-B/T-TP-FP

### @LVDS cable

Part Number	Description
DC020003Y0L	H-CONN SET ZJX MB-LCD 14 WXGA+ (-1ch)

### @LVDS cable

Part Number	Description
DC02000870L	H-CONN SET ZJX MB-LCD 14 WXGA+ (-2ch)

### @RTC BATT

Part Number	Description
GC20323MX00	BATT CR2032 3V 220MAH MAXELL

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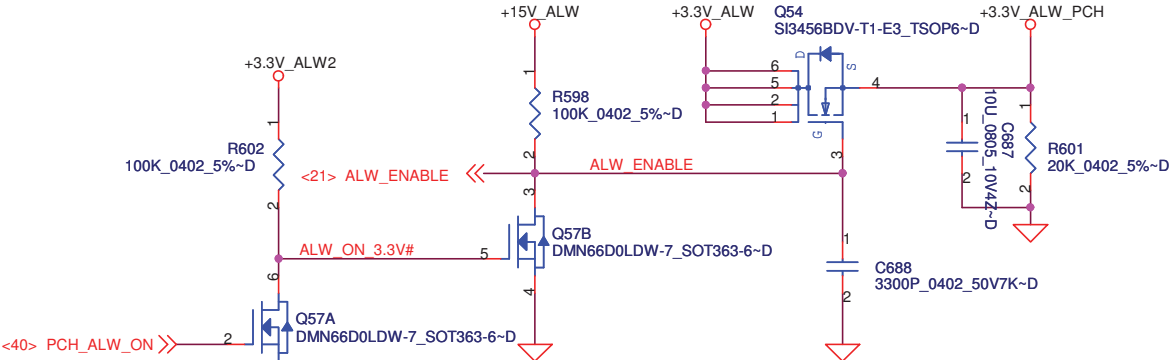
Title	Touch PAD/Int KB/LID
Size	Document Number
Date	Wednesday, January 20, 2010
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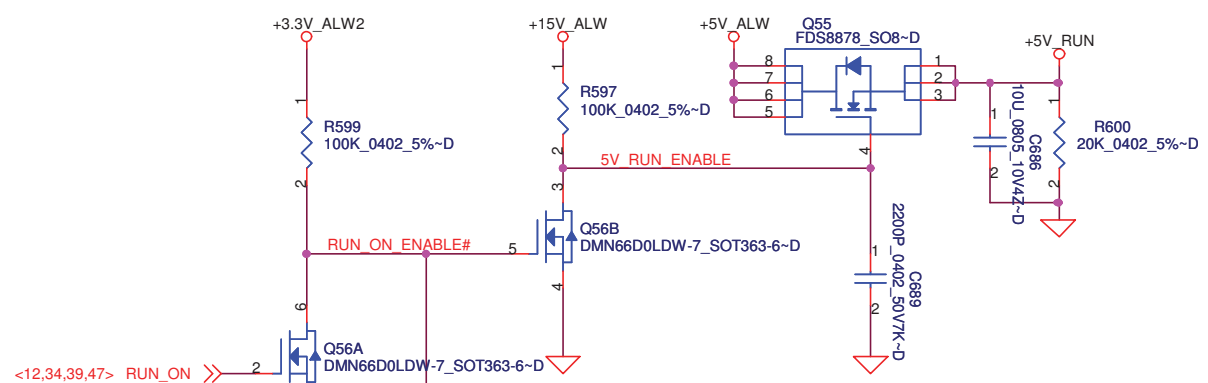
<http://laptop-motherboard-schematic.blogspot.com/>

DC/DC Interface

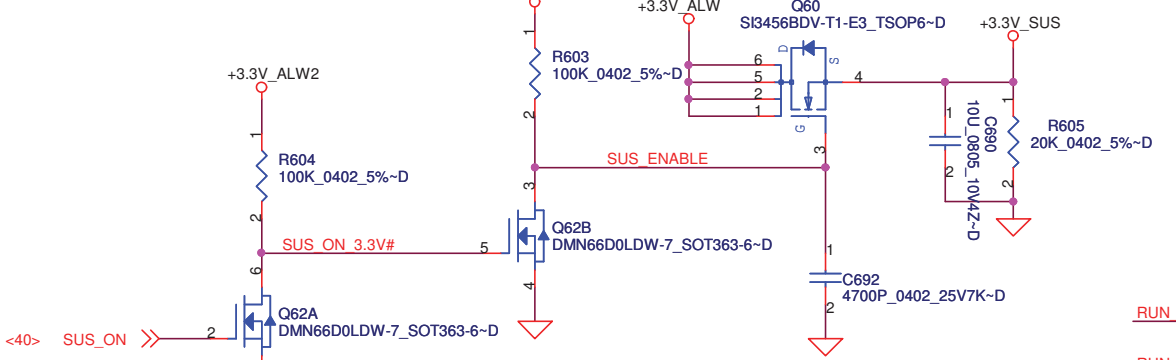
+3.3V\_ALW\_PCH Source



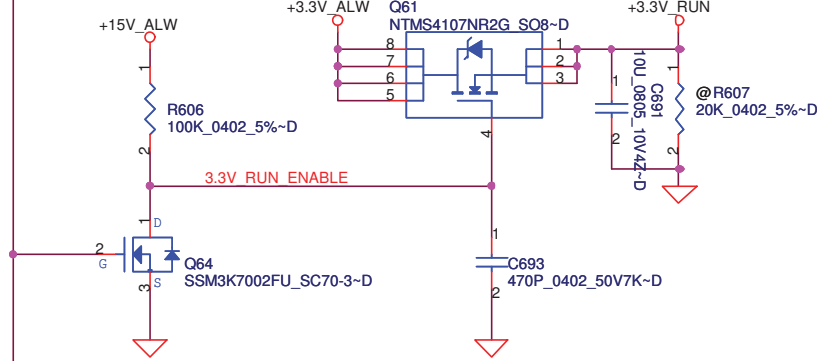
+5VRUN Source



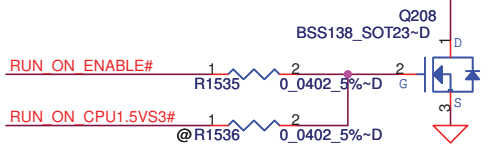
+3.3V\_SUS Source



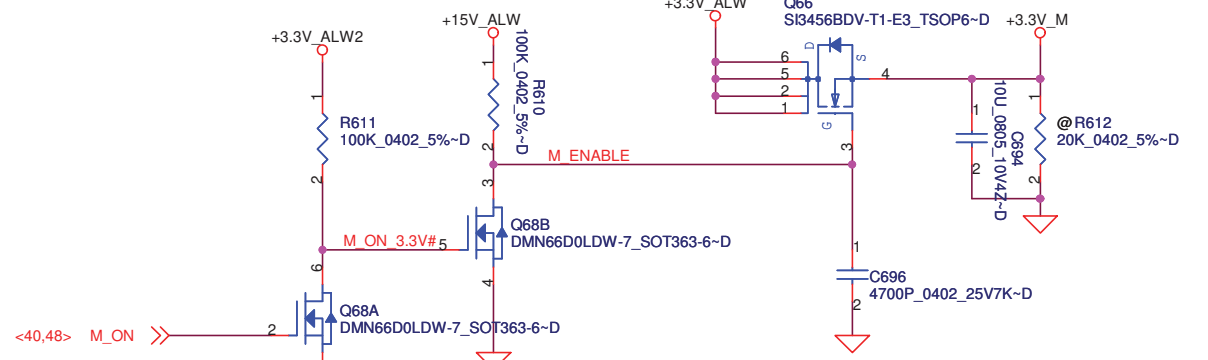
+3.3V\_RUN Source



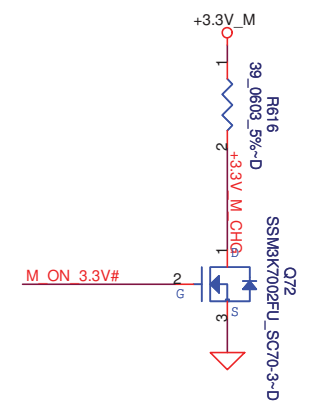
<8> 1.5V\_PWRGD >>> R1508 100K\_0402\_5%~D >>> 0.75V\_VR\_EN <47>



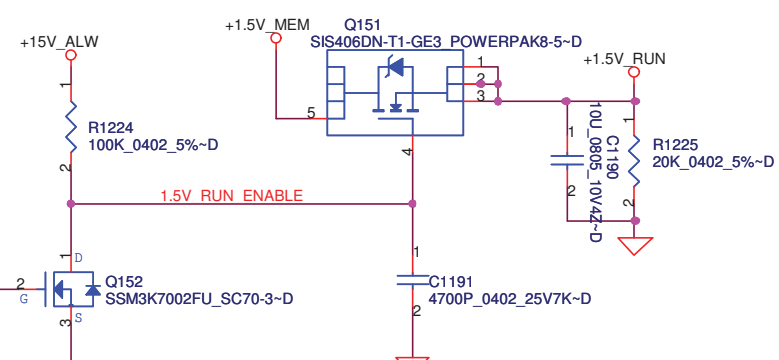
+3.3VM Source



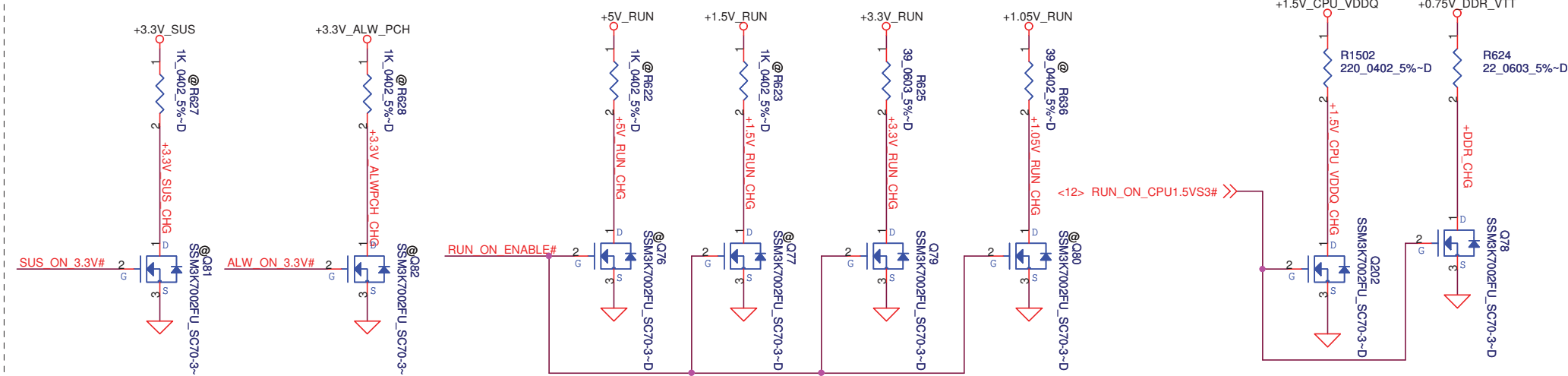
Discharg Circuit



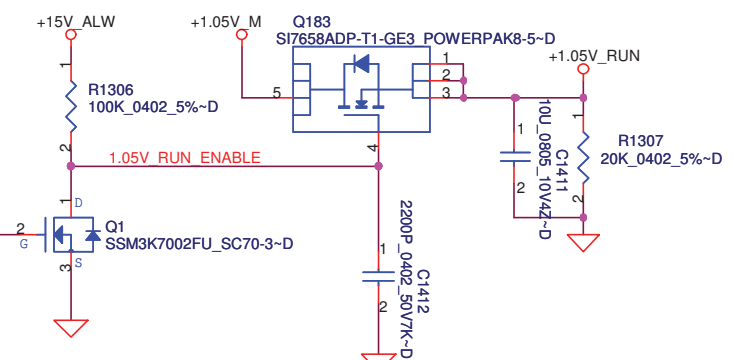
+1.5V\_RUN Source



Discharg Circuit



+1.05V\_RUN Source



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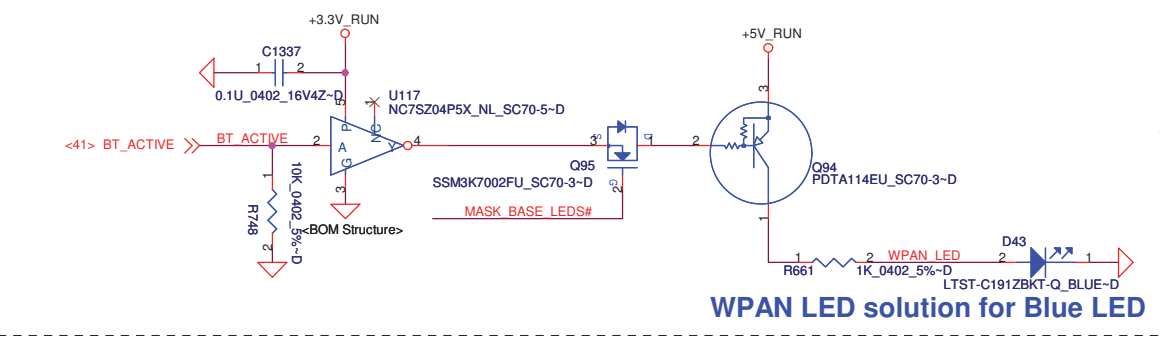
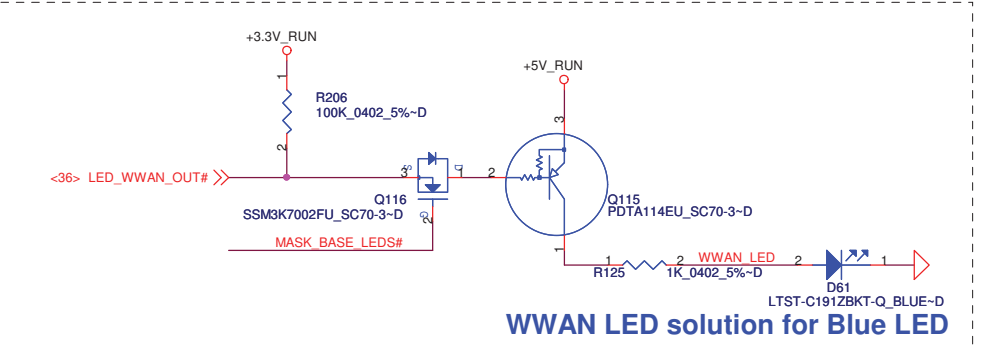
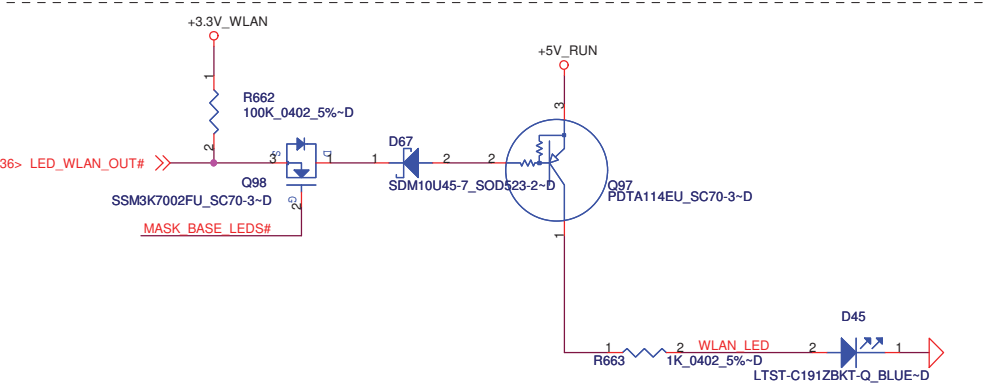
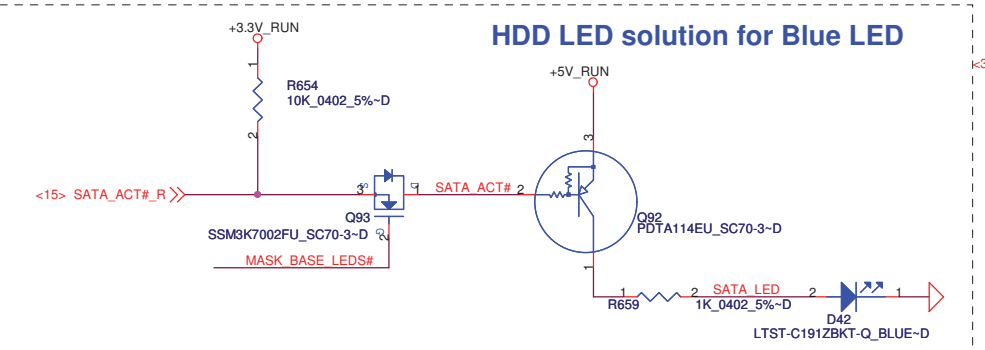
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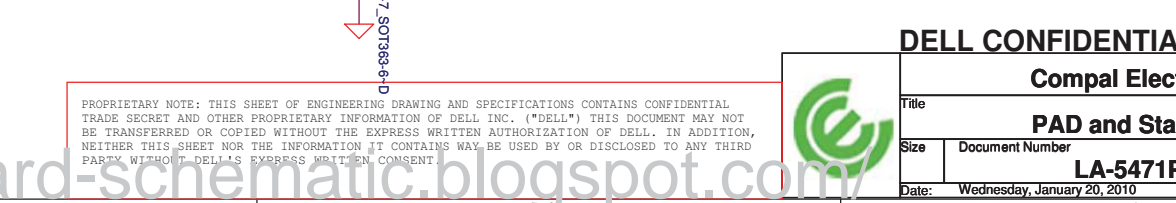
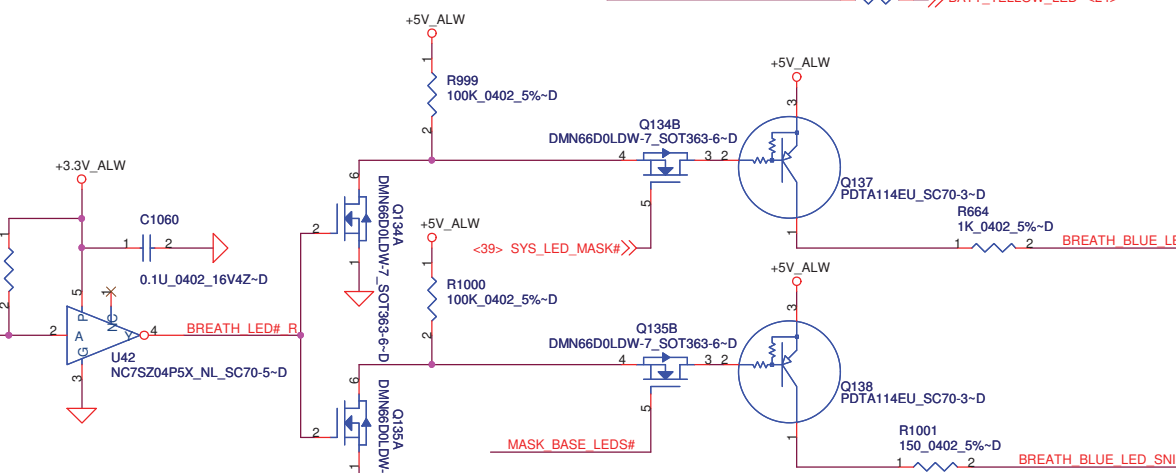
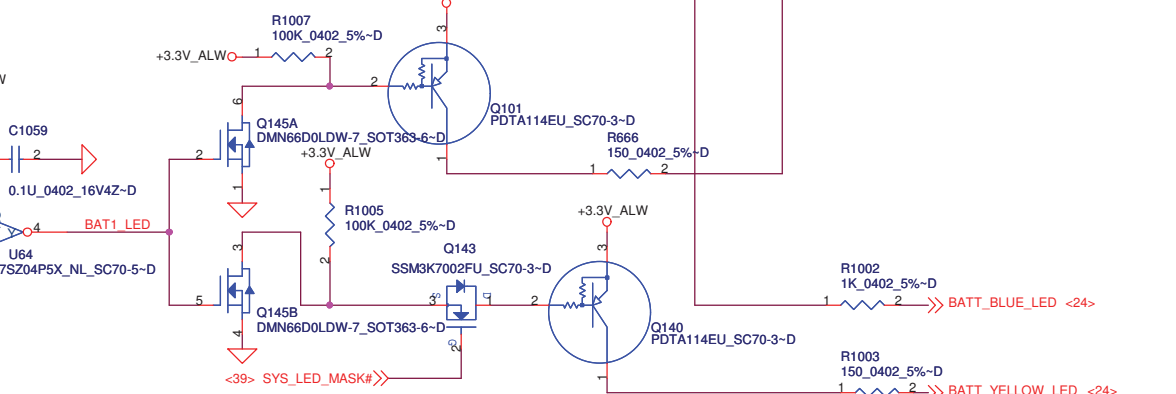
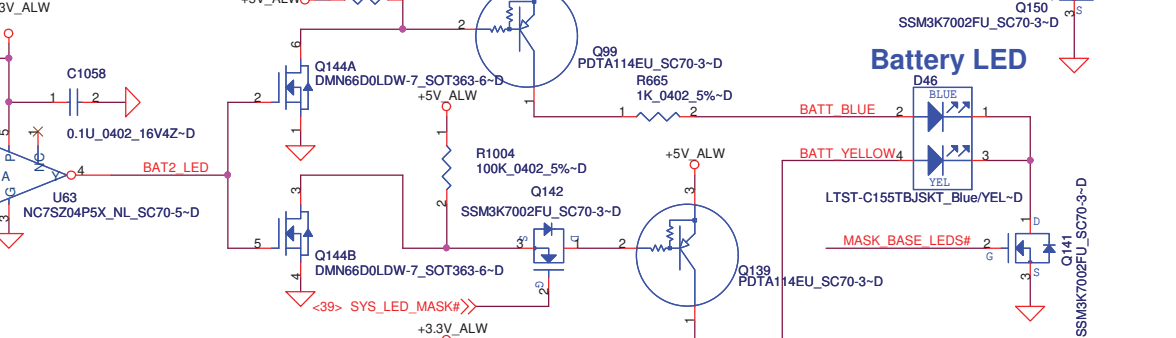
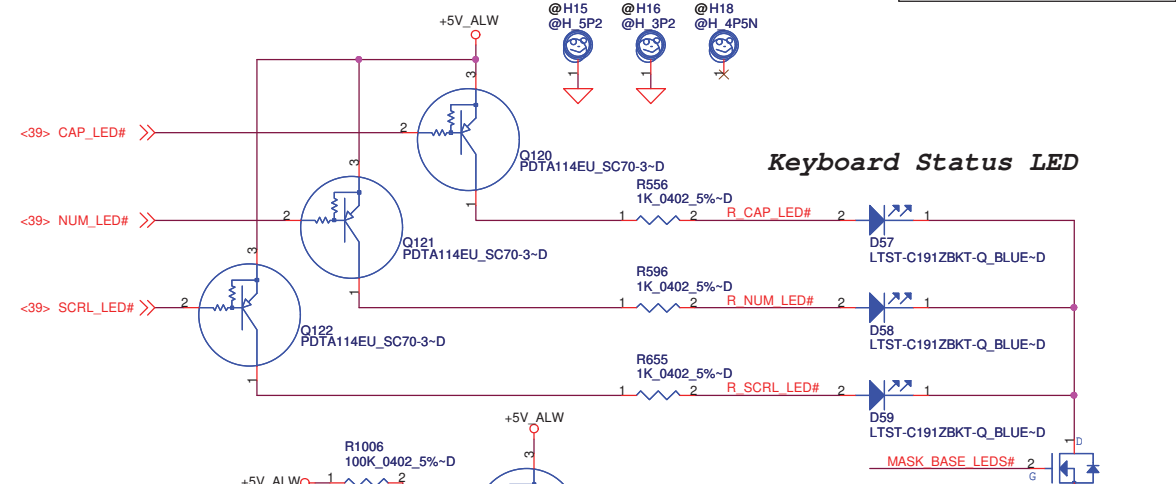
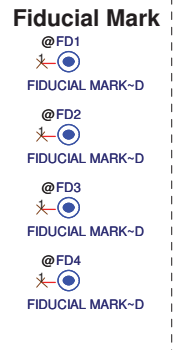
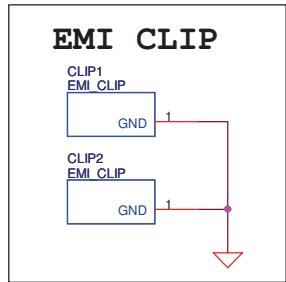
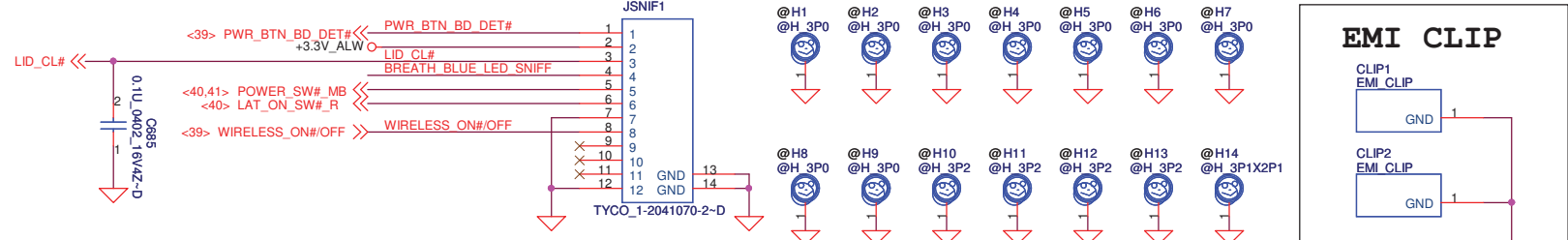
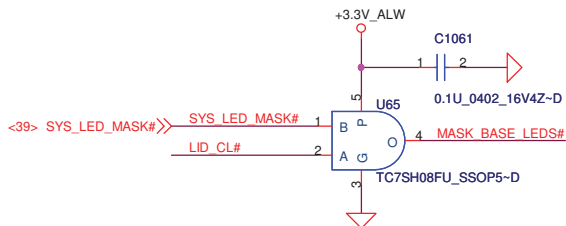
Title			POWER CONTROL	
Size	Document Number	LA-5471P		Rev 1.0
Date	Wednesday, January 20, 2010	Sheet	42	of 57

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LED Circuit Control Table		
	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Sniffer Function)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1



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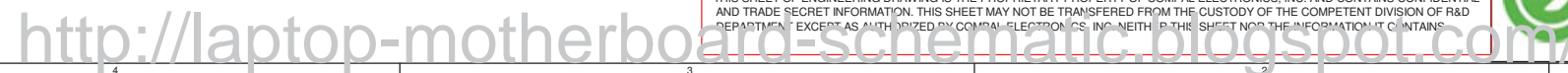
LA-5471P

Rev 1.0

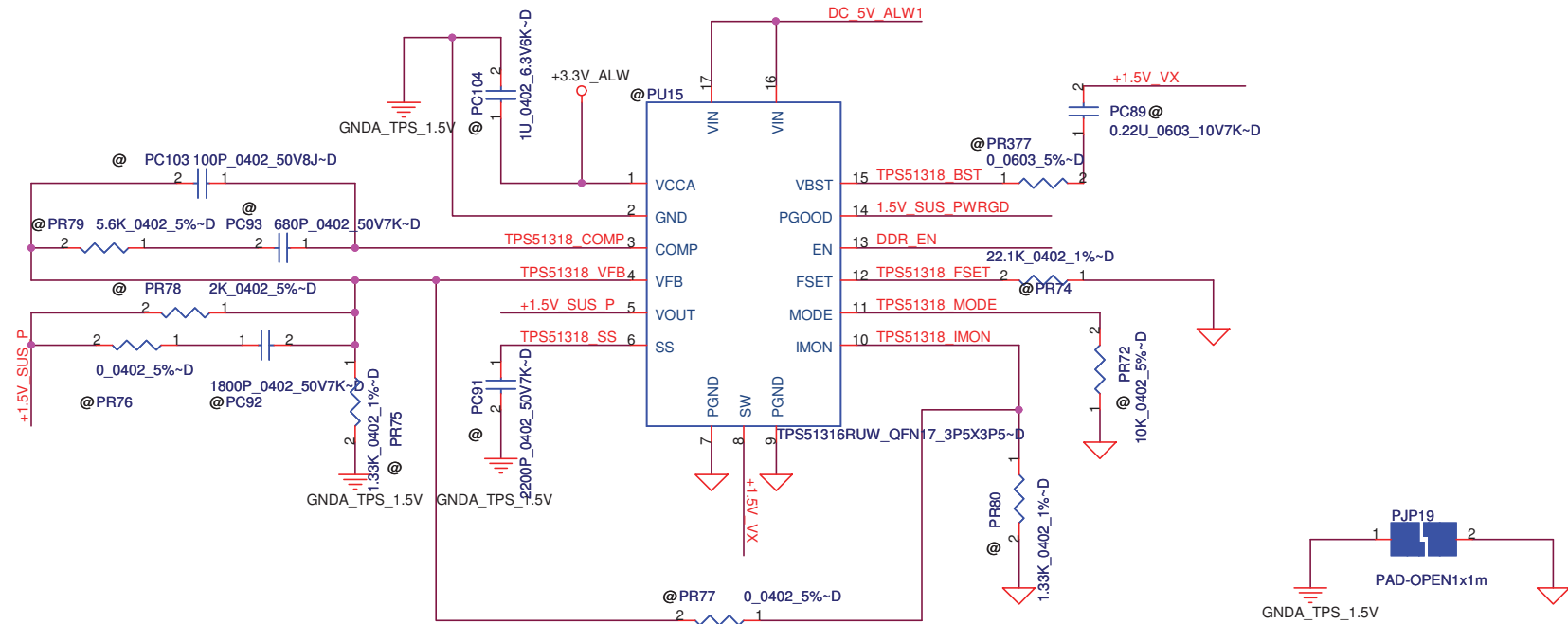
Date: Wednesday, January 20, 2010 Sheet 43 of 57





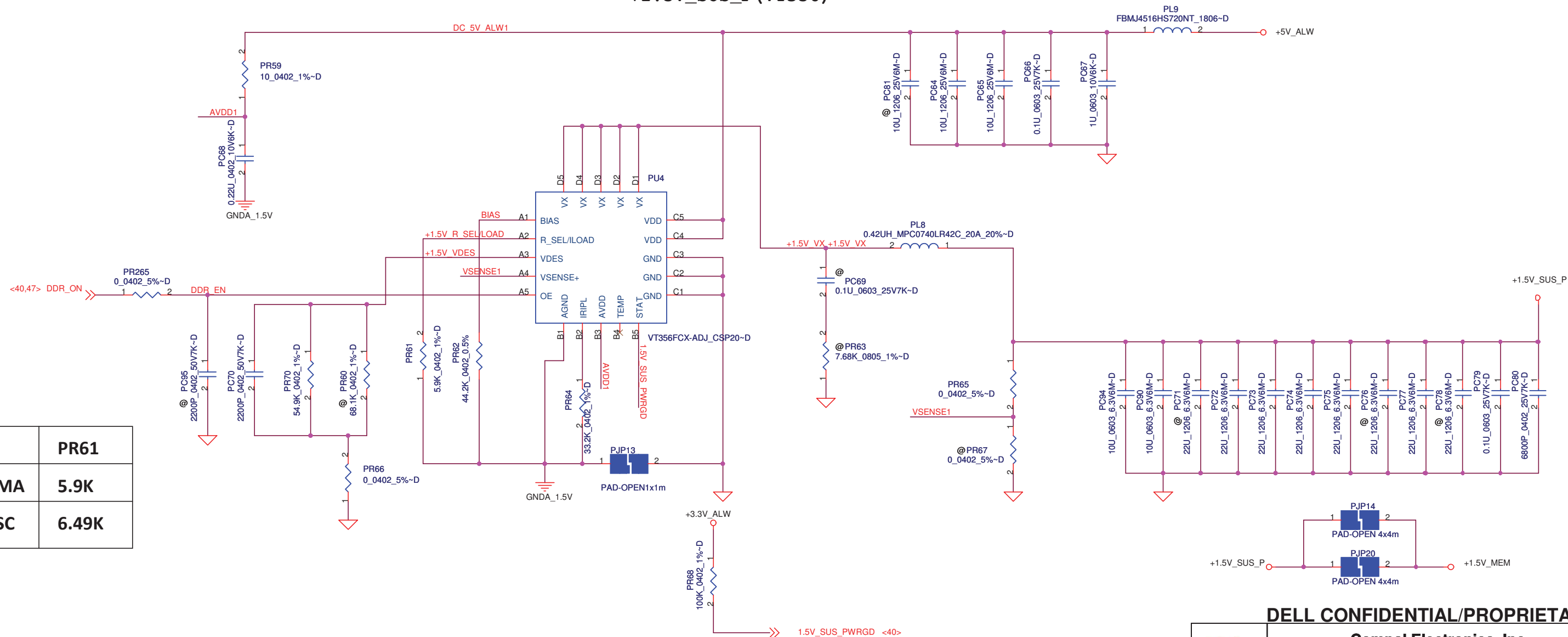
$$F_{sw} = 400\text{KHz}$$
$$F_{sw} = 300\text{KHz}$$


+1.5V\_SUS\_P (TPS51316)



1.5 Volt +/-5%  
Thermal Design Current : 5.828A  
Peak current : 8.326A  
OCP\_MIN :9.991A

+1.5V\_SUS\_P (VT356)



	PR61
UMA	5.9K
DSC	6.49K

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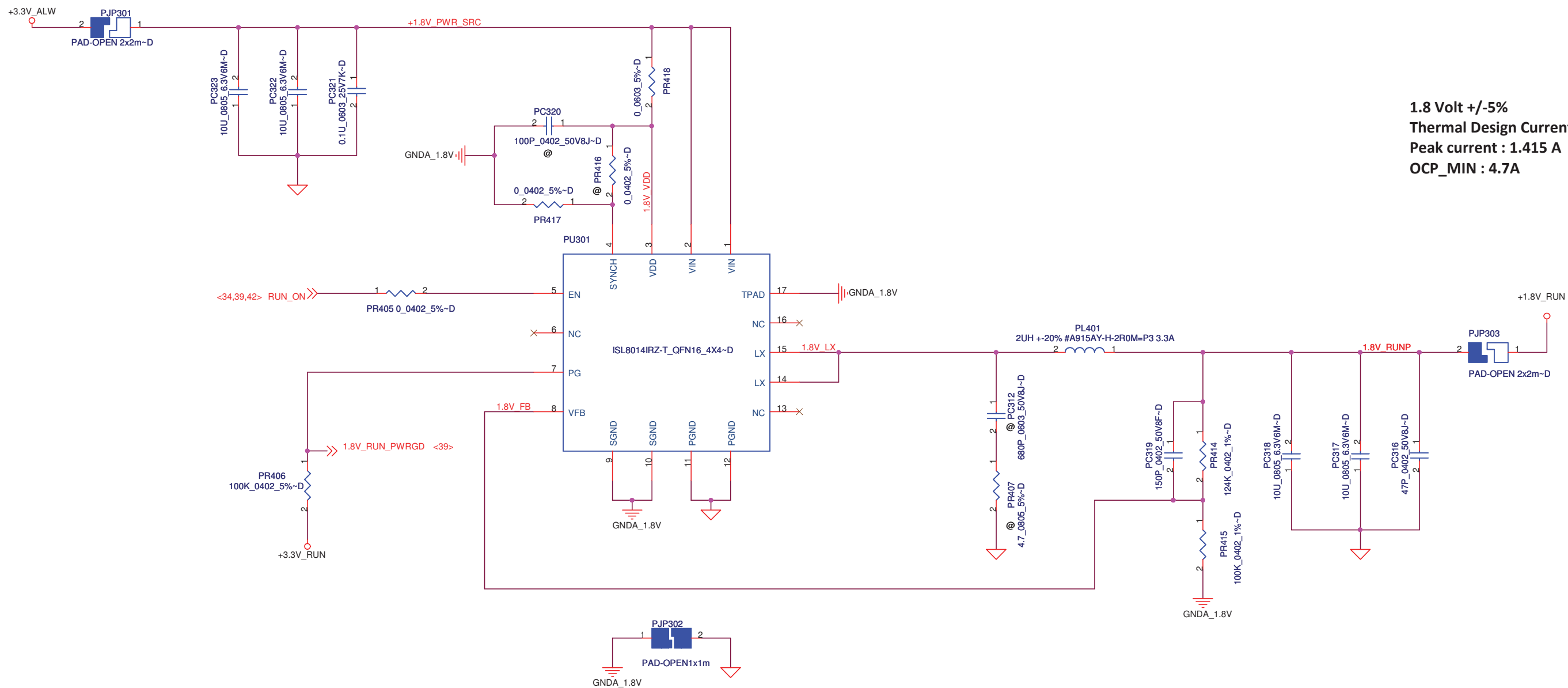
Compal Electronics, Inc.

+1.5V\_MEM

LA-5471P

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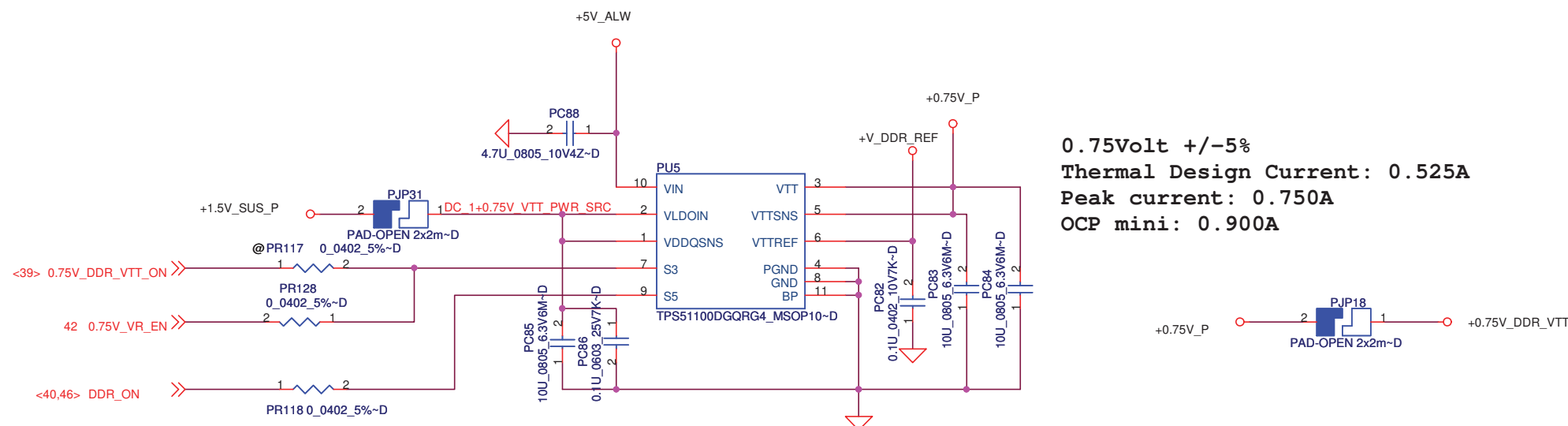
## +1.8V\_RUN



1.8 Volt +/-5%  
Thermal Design Current : 0.99A  
Peak current : 1.415 A  
OCP\_MIN : 4.7A

## +0.75V\_DDR\_VTT

### DDR3 Termination



0.75Volt +/-5%  
Thermal Design Current: 0.525A  
Peak current: 0.750A  
OCP mini: 0.900A

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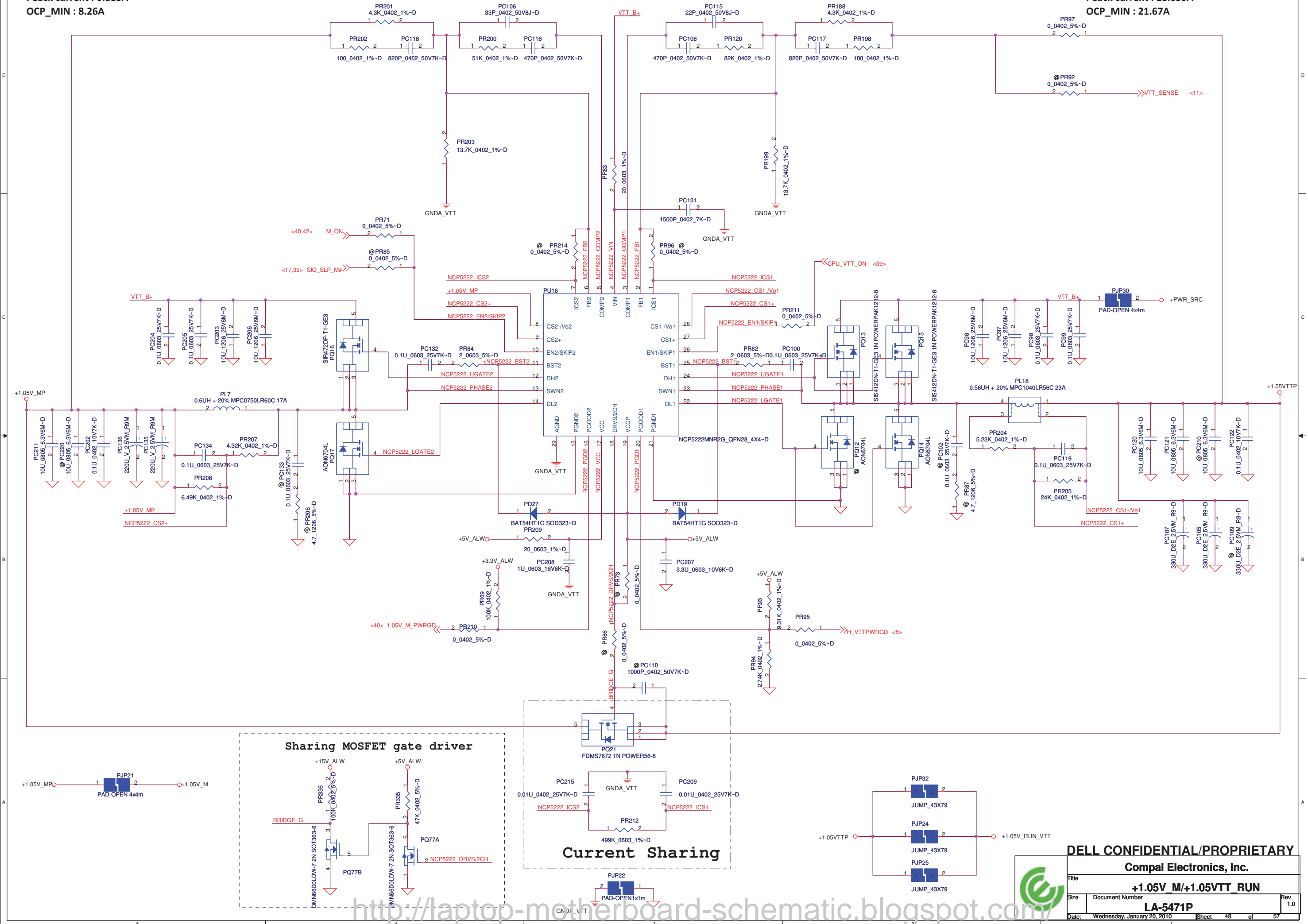
Title			
+0.75V DDR VTT/+1.8V RUN			
Size	Document Number		Rev
	LA-5471P		1.0
Date:	Wednesday, January 20, 2010	Sheet 47 of 57	

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1.05 Volt +/-5%  
Thermal Design Current : 4.818A  
Peak current : 6.883A  
OCP\_MIN : 8.26A

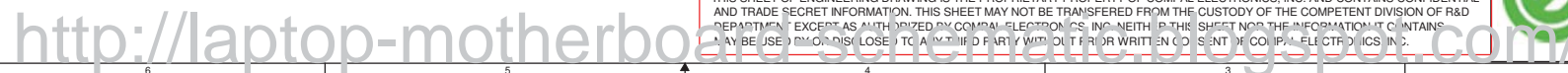
+1.05V\_M/+1.05VTT\_RUN

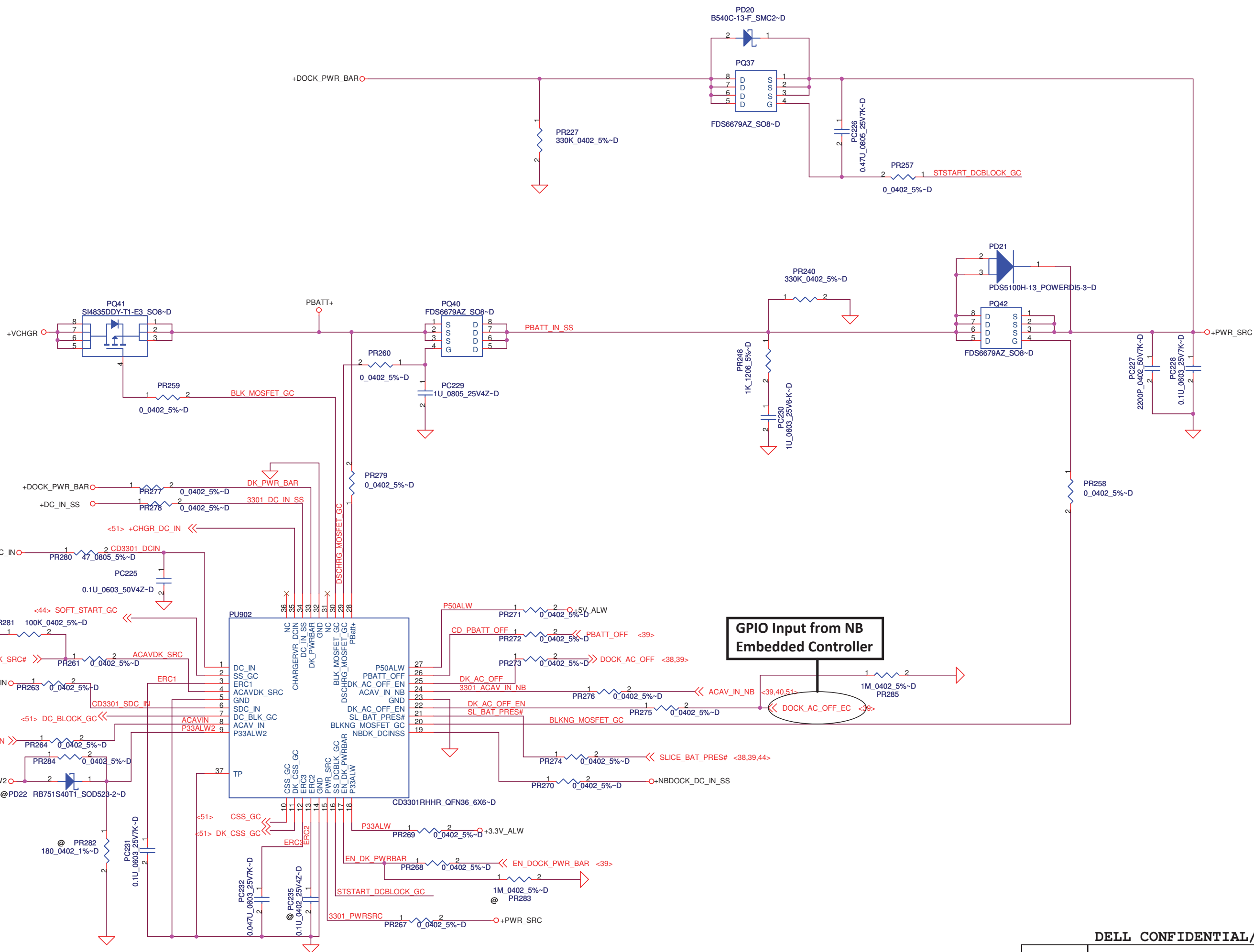
1.05 Volt +/-5%  
Thermal Design Current : 18A  
Peack current : 18.059A  
OCP\_MIN : 21.67A



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<b>Compal Electronics, Inc.</b>			
Title <b>+1.05V_M/+1.05VTT_RUN</b>			
Size	Document Number <b>LA-5471P</b>		Rev <b>1.0</b>
Date:	Wednesday, January 20, 2010	Sheet 48 of	57







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Selector

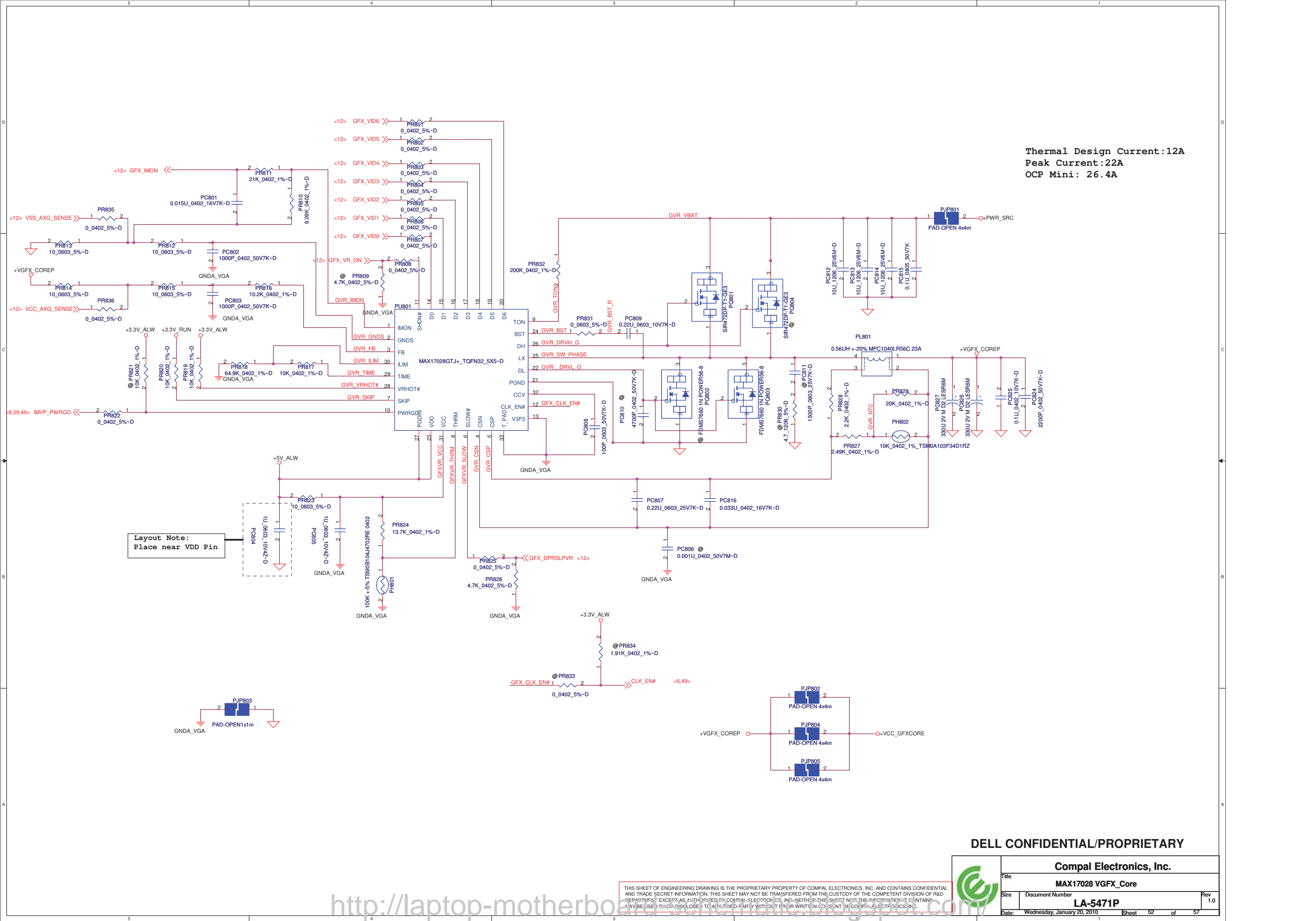
LA-5471P

Date: Wednesday, January 20, 2010 Sheet 50 of 57

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# Version Change List ( P. I. R. List )

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	40	HW	7/13/2009	COMPAL	Board ID	R98 change to 130k ohm	X01
2	30	HW	7/13/2009	COMPAL	follow M09 +3.3V_LAN enable control circuit	depop R47	X01
3	8, 12, 13, 42	HW	7/13/2009	Intel	Intel S3 reduction circuit.	Add R1469, R1497~R1505, R1507~R1509, C1875, C1878~C1884, Q199~Q202, Q205, Q207, Q208 , U141, PJP906, PJP907, change R879 to 1.5K, R880 to 750ohm, R624 to 22 ohm, change CPU CDDQ power source from +1.5V_MEM to +1.5V_CPU_VDDQ, change +.075_DDR_VTT discharge gate from RUN_ON_ENABLE# to RUN_ON_CPU1.5VS3#, add +1.5V_CPU_VDDQ discharge circuit, add net "DDR_HVREF_RST_GATE" from U36.A34 to Q119.2, "CPU1.5V_S3_GATE" from U36.A36 to R1501	X01
4	31	HW	7/22/2009	Broadcom	change C718 value	change C718 from .47uF to .22uF	X01
5	23	HW	7/22/2009	DELL	Follow DELL request to remove R3P circuit.	delete U140, R136, R138, R156,R507, R516, R519, R529, R531, R534~R536, R594, R1457, R1458, R1462, R1463, C434, C72, C73, C391, C406, pop R142, D2, C219	X01
6	41, 37	HW	7/22/2009	COMPAL	Per M09 lesson learn request	Re-define JTP1, JBI01	X01
7	19	HW	7/22/2009	Intel	GPIO1, 6, 7 need to PU if no used.	Add R1510, R1511	X01
8	40	HW	7/22/2009	COMPAL	Follow SMSC5045 spec	Add R1512, @C1885, C1886, change R560 to 100Kohm, add net name LAT_ON_SW#_R	X01
9	16	HW	7/22/2009	Intel	Intel Sighting report 3306048 to pop 25MHz crystal.	pop Y6, R685, C1168 (change to 18p), change R381 to C1887(18p)	X01
10	31	HW	7/22/2009	Broadcom	remove RFID disable circuit	remove R1062~R1065	X01
11	24	HW	7/22/2009	COMPAL	CAM Module change from 7pin to 8 pin.	change pin define for JEDP1	X01
12	31	HW	7/22/2009	Broadcom	R898 and R485 pop at the same time.	depop R898	X01
13	29	HW	7/29/2009	COMPAL	EMI solution.	change R1295 to L4 (220ohm) and R1215 from 22ohm to 47ohm.	X01
14	42	HW	7/29/2009	COMPAL	base on de-rating report.	change Q61 from AO4456 to NTMS4107	X01
15	36, 39	HW	7/29/2009	DELL	GPIO MAP update	Add connection from JMINI3.20 to 5028 pin A56, named "UWB_RADIO_DIS#"	X01
16	37, 39	HW	7/29/2009	DELL	GPIO MAP update	Add reserved R1513 between U95.18 and +3.3V_RUN, add R1514 between U95.18 and 5028.A47 named EN_ESATA_RPTR.	X01
17	42	HW	7/29/2009	COMPAL	resolve leakage issue.	Pop R625 and Q79, change R625 to 0603 size.	X01
18	31	HW	7/29/2009	Broadcom	resolve 5882 leakage issue	add R1515, Q209, Q210	X01
19	26	HW	7/29/2009	COMPAL	resolve 8200 DVI can't work issue.	add R1516	X01
20	31	HW	7/29/2009	Broadcom	resolve smart cart can't work problem.	pop R775, R537, depop R776.	X01
21	36	HW	7/29/2009	COMPAL	Correct PU power rail for USB_MCARD1_DET#	change USB_MCARD1_DET# PU to +3.3V_RUN	X01
22	31	HW	7/29/2009	COMPAL	remove R1061 to avoid double PU and provide back-drive path.	remove R1061	X01
23	19	HW	7/29/2009	COMPAL	add PD to provent floating at PCH GPIO22, GPIO34.	add R1520, R1521	X01
24	21	HW	7/29/2009	COMPAL	Follow the pop option on CRB1.6 to depop C39 for +VCCACLK, C610 for +SATAPLL, C111 and C112 for +1.05V_M_VCCEPW	de-pop C610, C39, C111, C112	X01
25	37	HW	7/31/2009	DELL	correct the connection for EN_ESATA_RPTR. it's not detect function.	change the connection from U95 Pin18 to Pin7	X01
26	27	HW	8/05/2009	COMPAL	base on EA and EMI test result on RGB	change L61~L63 to BLM18BB050SN1D and C390, C518, C996, C251~C253 to 4.7p	X01
27	36	HW	8/05/2009	COMPAL	change the PU to +3.3V_RUN refer to the core power rail at PCH side.	change the PU for R458 from +3.3V_ALW_PCH to +3.3V_RUN	X01
28	18, 35, 36	HW	8/05/2009	DELL	Braidwood no longer support on Rothschild.	Delete NVM connection, delete R1411, R1452, R1453, <del>R866, R872</del> , JBW1, C1851, C1852. Move JMINI1 power circuit to page 36.	X01
29	10	HW	8/06/2009	Intel	Follow Intel recomment to add debug TP.	Add T186~T190	X01
30	28	HW	8/06/2009	COMPAL	Follow M09 to change the PU to +3.3V_RUN	Pop R1239 and change the PU power rail from +5V_MOD to +3.3V_RUN	X01
31	31	HW	8/06/2009	Broadcom	Follow Broadcom request	delete T159, R494, R498, R631, R634, R898, C640, C641, C642 C647, C1026, L73, add R1522, C1887, C1888, change connection for R496, R497 to GND, change connection for JCS1 pin3 and pin4.	X01
32	23	HW	8/12/2009	COMPAL	FAN1_DET# should have 10K PU to +3.3V_M	add R1517	X01
33	40	HW	8/12/2009	SMSC	per AN 19.6 (section 6.7, page 19)	change R541, R554, R1512 from 1K to 10K.	X01
34	23	HW	8/12/2009	SMSC	The pull-up source of the R150 should be changed to +VCC_4002 by SMSC request	change R150 PU from +3.3V_M to +VCC_4002	X01
35	23	HW	8/12/2009	SMSC	Add discharge ckt for+3.3V_M, watch dog timer may not be resetED when EMC4002 VDD_PWRGD is not completely at Logic Low.	pop Q72 and R616, change R616 from 1K(0402) to 39ohm(0603)	X01
36	8	HW	8/12/2009	COMPAL	Follow Margaux to fix S3 power up sequence.	change C1880 from 0.01uF to 0.22uF	X01

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
37	21	HW	8/12/2009	Intel	WW30 Calpella MoW, Intel request change L45 & L46 to 10uH, DCR=0.36 ohm	change L45, L46 from 10UH_LB2012T100MR_20% to 10UH_LBR2012T100M_20%	X01
38	26, 38	HW	8/12/2009	Intel	Per Intel check list rev1.6, change PD value of HPD signals from 100K to 110K ohm.	change R186, R191, R796, R798 from 100Kohm to 110Kohm	X01
39	39	HW	8/12/2009	COMPAL	VGA_ID_DISC and VGA_ID_UMA should pulled up to +3.3V_ALW	change PU from +3.3V_RUN to +3.3V_ALW for R875, R881	X01
40	31	HW	8/13/2009	Broadcom	Base on Broadcom review for Margaux.	add @R1523, R1524, change C718 to 470nF, C646 to 220nF.	X01
41	15, 30, 33, 40	HW	8/13/2009	COMPAL	Base on EA result for all X'tal and OSC.	change C296, C297 to 12pF, C476 to 33pF, C427 to R1526(200ohm), C674&C675 to 33pF, R421 to 100ohm	X01
42	8	HW	8/13/2009	Intel	Refer to Intel S3PowerReduction_whitePaper_Rev0.9	add R1525 and C1890	X01
43	33, 34	HW	8/13/2009	Ricoh	Correct the Cardbus Controller to R5U242 on PT phase.	change R46 to C1889, C21 from 10uF to 47uF, correct symbol to R5U242	X01
44	30	HW	8/14/2009	Intel	bsae on Intel review result.	remove +LOM_VCT, R562, C41, depop C712 and change the net name to +LOM_VCT_IO, add C1891	X01
45	19, 37	HW	8/14/2009	COMPAL	GPIO MAP update for EN_ESATA_RPTR#.	add @R1528, @Q211, pop R1513, depop R1514, change net name from GPIO16 to EN_ESATA_RPTR#	X01
46	8, 40	HW	8/14/2009	COMPAL	GPIO MAP update for CPU_DETECT#	Add R1529, delete TP1, connect JCPU.AH24 to U36.B18	X01
47	37	HW	8/17/2009	COMPAL	Base on EMI team request to reserve command choke for test	Add L90, L91, @R1530~ @R1533, change L64 to 2@, depop R791, R792.	X01
48	30	HW	8/17/2009	Intel	bsae on Intel review result.	reserved R1534.	X01
49	42	HW	8/18/2009	COMPAL	reserved pop option to improved S3 circuit.	add R1535, @R1536	X01
50	31	HW	8/18/2009	COMPAL	base on Smart card EA result.	R772 to 47 Ohm and C1015 to 10pF	X01
51	28, 37	HW	8/18/2009	COMPAL	base on SATA EA result on HDD and ESATA	depop R1308, R1298, pop R1304, R1031	X01
52	26	HW	8/20/2009	Pericom	Per Pericom: Add 100pf to GND between the source and 8200	add C1893, C1894	X01
53	26	HW	8/20/2009	COMPAL	reserved for debug.	reserved R1537~R1539	X01
54	16	HW	8/21/2009	COMPAL	Base on EA result on Crystal.	change Y6 to SJ100006M0L (CL=12P)	X01
55	29	HW	8/21/2009	COMPAL	Base on Vender suggestion	change X4 to SiTime 12MHZ_15PF_SIT8102AC3333E12T	X01
56	36	HW	8/23/2009	COMPAL	Follow EA result	add R1540~R1542	X01
57	24	HW	8/23/2009	COMPAL	follow eDP specification.	delete R279 and R1027	X01
58	21	HW	8/24/2009	COMPAL	base on EA result to solve SATA eye.	delete R557	X01
59	13, 14	HW	8/25/2009	COMPAL	Base on EMI request to pop the caps at DDR DIMM for verify.	pop C1121~1124, C1145~C1148	X01
60	42	HW	8/25/2009	COMPAL	Double discharge path on +3.3V_M, +3.3V_RUN and +1.5V_CPU_VDDQ	de-pop R607, R612 and R1498	X01
61	30	HW	8/26/2009	Intel	Follow Intel WW35 '09	Change R1526 to C427 10pF and change C475 to 33pF	X01
62	40	HW	10/06/2009	COMPAL	Board ID	Change R98 to 33K	X02
63	29	HW	10/06/2009	IDT	Follow IDT request to add a filter circuit	Change R340, R342, R1041, R1042 to 2K, add C1895~1898 (1000p), depop C1066, C1067	X02
64	17	HW	10/06/2009	COMPAL	add level shift for CRT DDC signal	add Q212, @1543, @1544	X02
65	32	HW	10/06/2009	COMPAL	Follow Intel DG FLEX clock topology.	change R910 to 22ohm.	X02
66	17	HW	10/06/2009	COMPAL	Follow Schematic check llist rev2.0	change R268 from 1Kohm to 10Kohm, depop C105, C106	X02
67	36	HW	10/06/2009	COMPAL	Correct the PU power rail for USB_MCARD2_DET#	change R447 PU from +3.3V_RUN to +3.3V_ALW +3.3V_ALW_PCH	X02
68	36	HW	10/06/2009	COMPAL	layout request to reduce stub.	add R1545, R1546.	X02
69	16	HW	10/21/2009	COMPAL	Follow X'tal EA. BIT number:DF346635	change C1168 C1187 from 18pF to 12pF.	X02
70	31	HW	10/27/2009	COMPAL	Follow Broadcom RFID final value.BIT number:DF341072	change L71/L72 from 150nH to 68nH, C1070/C1071 from 750pF to 1500pF, C1887/C1888 to 150pF	X02
71	16	HW	10/29/2009	COMPAL	Follow new SMBUS topology to solve AMT Memory issue.	add R1547, R1548	X02
72	41	HW	11/04/2009	COMPAL	Follow new TP spec	change PU for R613 and R614 from +5V_ALW to +3.3V_ALW	X02
73	24	HW	11/04/2009	COMPAL	Solve DF344566 EMI test fail at 200MHz from PCH PCI noise	change R166 to L92 (220ohm 0603 size bead)	X02
74	31	HW	11/04/2009	Broadcom	U34 has been validated to support both Atmel/Numonyx dataflash devices to meet Dell two sources requirement.	remove U14.	X02
75	31	HW	11/05/2009	COMPAL	W25X32VSSIG EOL	change U13 from W25X32VSSIG to W25Q32BVSSIG	X02
76	36	HW	11/05/2009	COMPAL	support WiMAX LED.	pop R840	X02
77	8, 28	HW	11/05/2009	COMPAL	reduce SMBUS stub.	add R1549~R1552 as no pop.	X02
78	40	HW	11/11/2009	COMPAL	solve RTC timing issue and follow the newest EA result.	change C675 from 33pf to 39pf and Y1/4 from 1TJS125DJ4A420P to Q13MC30610018 (10ppm)	X02
79	24	HW	11/11/2009	COMPAL	follloe LCD timing EA result.	change R161 from 470ohm to 100ohm.	X02
80	24	HW	11/11/2009	COMPAL	ME_FWP and SIO_EXT_WAKE# are OD pin.	add R1557 2.2Kohm PU to +3.3V_ALW_PCH , R1558 10K PU to +3.3V_RUN	X02

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
81	21	ESD	11/17/2009	COMPAL	Solve TP ESD issue. DF349471	add R1564, R1565 (100ohm) to replace L41 and L42	X02
82	19	HW	11/17/2009	Intel	Follow check list rev2.0 to add the PU for GPIO22, GPIO34	change the R1520, R1521 from PD to PU +3.3V_RUN	X02
83	31	HW	11/17/2009	COMPAL	use the same solution on Smart card clock.	change R772 from 47ohm to 22ohm.	X02
84	31	HW	11/18/2009	COMPAL	check list rev2.0 requirment	change R224 tolerance from 5% to 1%.	X02
85	40	HW	12/22/2009	COMPAL	Change board ID for X'build	change R98 from 33k ohm to 1k ohm.	A00
86	37	HW	12/22/2009	COMPAL	For DFB concern, change JBIO1 footprint	change JBIO1 footprint from TYCO_1734242-6_6P-T to TYCO_2041070-6_6P .	A00
87	38	EMI	12/22/2009	COMPAL	Solve Simplo battery slice EMI issue	Add C1900 and reserved C1899	A00
88	36	HW	12/22/2009	COMPAL	Solve Wi-max LED abnormal operation	De-pop R1409	A00
89	31	HW	12/22/2009	COMPAL	SC_CLK damping resistor keep PT value	change R772 from 22ohm to 47ohm.	A00
90	12	HW	12/23/2009	COMPAL	Surge voltage on UMA GFX core	change R358 from 4.7k ohm to 470 ohm.	A00
91	31	HW	12/23/2009	BRCOM	By BRCOM recommand	Change L71,L72 from 68nH to 150nH, C1070,C1071 from 1500pF to 390pF,C1887, C1888 from 150pF to 390pF.	A00
92	32	HW	12/23/2009	COMPAL	Change TCM to T1 version	Change TCM from SSX44B-D-T to SSX44-D-T1	A00
93	8, 15	HW	1/5/2010	COMPAL	cost saving for XDP,JTAG	De-pop R780~R785, R22, R24, R1241, R3, R6, R7, R19, R68, R1153, R1156, R1157, R66, C19, C20, <del>R123, R804, R805, R806, R807, R1281, R1282, R1315</del>	A00
94	33, 34	HW	1/5/2010	RICOH	CardBus change from ES2 to ES3	Change U94 from SA00003C21L to SA00003C22L	A00
95	39	HW	1/7/2010	COMPAL	RF team request to add 0.1uF capacitor on +5V_RUN of JTS1 to reduce 1811.5MHz noise	Add C114 on +5V_RUN of JTS1 for ATG configuration	A00
96	28, 37	HW	1/15/2010	COMPAL	Change SATA repeater material to power saving part	Change U95 and U96 part number to SA00003P10L	A00
97	26	HW	1/19/2010	Pericom	Pericom DP SW DP8200 has new silicon W version in stead of Y version	Change U9 to SA00003CD2L	A00
98	11	Acoustic	1/19/2010	COMPAL	To reduce acoustic noise	De-pop C53 and C54	A00

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	50	Selector	7/20	TI	CSS GC logic wrong issue	Add PR282 180_ohm to GND	X01
2	46	1.5V_MEM	7/20	Compal ADC Guangyong	Add droop resistor for TI solution	Add PR77	X01
3	45	+3.3V/+5V	8/17	Compal ADC Guangyong	Change 3V/5V choke for cost down	change PL5 from SH00000H90L to SH00000FN0L change PL6 from SH00000HB0L to SH00000HR0L	X01
4	50	Selector	8/17	Compal	Add 1M_ohm pull down to fix ACAV_IN_NB oscillation when battery mode S5	Add PR283	X01
5	50	Selector	8/17	TI	new version CD3301 (PG2.1) don't need PD22 and PR282	depop PD22 add PR282, pop PR430	X01
6	50	Selector	8/17	TI	DOCK_AC_OFF_EC floating issue	add PR285	X01
7	49, 52	+VCORE +VGFX_CORE	8/17	Compal	change thermistor package from 0603 to 0402 for cost down	Change PH3,PH4,PH5 and PH802 from SL200000B0L to SL200000W0L	X01
8	47	1.8V_RUN	8/18	MAXIM	Output ripple voltage unstable issue	<del>Change PC314 from SE00000868L(22u/0805) to SE00000000L(100u/1206) Change PR409 from SD03480618L (8.06k) to SD03460418L (6.04k) Change PR410 from SD03440218L(4.02k) to SD03430118L(3.01k) Change PR408 from SD014402A8L(40.2 Ohm) to SD000008H8L(51 Ohm) Change PC315 from SE000003W8L(820pF) to SE076333K8L (3300pF) Change PR411from SD000000268L(6.98K) to SD03445318L(4.53K) Change PC310 from SE074102K8L(1000P) to SE074472K8L(4700pF) Change PC309 from SE071330J8L (33pF) to SE071560J8L (56pF) Change PC311 from SE042104K8L(.1u/0603/25V) to SE076104K8L(.1u/0402/16V) Add PR413 SD02800008L (0 Ohm)</del>	<del>X01</del>
9	52	Vcc_gfx_core	8/19	Compal	Low side Vds ring over SPEC	Change PQ802 and PQ803 from SB00000KP0L(BSC882N03MS) to SB00000KM0L(FDMS7660)	X01
10	52	Vcc_gfx_core	8/20	Compal	Fine tune Imon time constant meet Intel SPEC 300uS~500uS	Change PC801 from SE068103K8L(0.01uF) to SE076153K8L(0.015uF)	X01
11	52	Vcc_gfx_core	8/20	Maxim	Fine tune transient RC time constant	Add PC816 SE076333K8L (0.033uF)	X01
12	49	+VCORE MAX17030	8/20	Maxim	Vcore FDIM issue	Change PR102, PR103 and PR104 from SD013220B8L(2.2) to SD00000V98L (1.1) Change PR310, PR311 and PR312 from SD03430118L(3.01k) to SD03424918L(2.49k) Change PR307, PR308 and PR309 from SD03422118L(2.21k) to SD03417418L(1.74k) Change PR137 from SD03449910L(4.99k) to SD03447518L(4.75k) Add PC271,PC272 and PC273 SE075223K8L(0.022uF)	X01
13	48	+1.05VM/ +1.05VTT	8/20	ON	Fine tune DC accurcay	Change PR188 and PR201 from SD03451018L(5.1k) to SD00000U28L(4.3k) Change PR199 and PR203 from SD03416228L(16.2k) to SD03413728L(13.7k) Change PR198 from SD03468008L(680 Ohm) to SD03418008L(180 Ohm) Change PR202 from SD03468008L(680 Ohm) to SD03410008L(100 Ohm) Change PC108 and PC116 from SE074331K8L(330p) to SE074471K8L(470p) Change PR200 from SD00000DM0L(200k) to SD03451028L(51k) Change PC115 from SE071300J0L(SE071300J0L) to SE071220J8L(22P) Change PC106 from SE071300J0L(30P) to SE071330J8L(33P) Change PR204 from SD03447518L(4.75K) to SD03452318L(5.23K) Change PR205 from SD03444228L(44.2K) to SD03424028L(24K) Change PR207 from SD00000LZ0L(3.83K) to SD00000J20L(4.32K) Change PR208 from SD03482518L(8.25k) to SD03464918L(6.49k)	X01



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